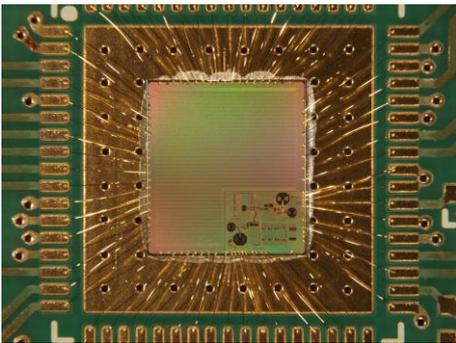


# Single-chip\* for low-cost high-precision positioning



Picture of die (size 4.5 x 5 mm<sup>2</sup>)

The chip includes analog front-end and digital baseband and supports the processing of a large number of GNSS signals. It can synchronously and simultaneously process the following systems and signals:

- GPS L1 C/A
- GPS L5
- GLONASS G1 (L1OF FDMA)
- Galileo E1 open service<sup>1</sup>
- Galileo E5a<sup>1</sup>

<sup>1</sup> Compatible to IOV-Galileo-Satellites

## Main benefits

- High-precision without any correction data: *~1 m absolute accuracy* (ionospheric error correction through reception of two frequencies)
- Low-cost: scalable for mass market applications
- Robust and reliable positioning solution in challenging reception environments (e.g. residential areas, urban canyons)
- Energy-efficient design
- Well suited for small form factor devices

## Application examples

- Automotive, e.g. e-call or Advanced Driver Assistance Systems
- Personal Navigation Devices, e.g. Location Based Services
- Machine control, e.g. precise farming, rail transport
- Asset tracking

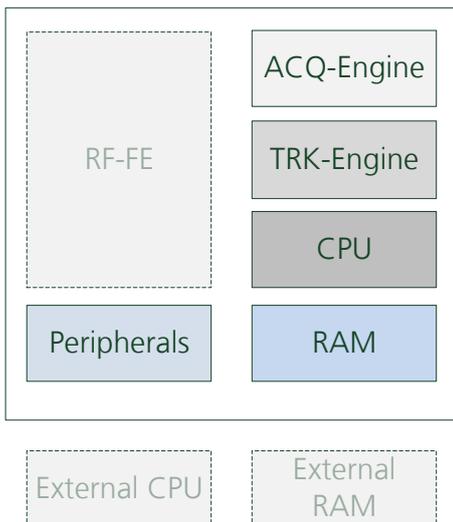
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*IP block diagram with integrated RAM  
(the radio frequency front-end (RF-FE) is also  
included and completes the mixed signal ASIC  
approach)*

## Technical details

- Clock reference adjustable in the range of 10 to 75 MHz
- Sleep-mode, adaptive clock and power management for low power consumption
- Software deactivation for circuit parts, e.g. acquisition engine or tracking channels
- Support for passive antennas: integrated LNAs (lower and upper frequency bands)
- Acquisition sensitivity: better than -145 dBm
- Acquisition engine with 16 k FFT
- Free GNSS and frequency selection for each tracking channel
- 40 tracking channels with 5 complex correlator outputs each
- Integrated processor for PVT solution at high output rate (50 Hz)
- 1 MB on-chip program-RAM
- Supports different output formats including NMEA
- Supports SD cards as boot medium
- RTK support with external CPU
- External memory with external memory code supported
- SPI master controller on-chip
- Dual UART interface
- 7 to 10 UGPIOs available
- Supply voltage 1.3 V core and 1.8 V pad
- QFN 68 package

## Modular IP core licensable

- Scalable processor
- Configurable General Purpose Memory Controller
- DMA transfers
- Number of tracking channels and user peripherals
- Support for customer-specific CPUs

## Collaboration

The IP core has already been implemented as a prototype in a TSMC 65 nm technology (see picture of SoC, page 1) and is available on a prototyping platform. Fraunhofer IIS presents the IP core with the aim of engaging partners for further development as well as for production and licensing.

The digital design exclusively uses standard logic cells and no technology specific components. All internal RAMs have standard interfaces which are summarized in a library and can be adapted to the needs of any technology.