Fraunhofer
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# AFE13b010kS180nm

Ultra-Low-Power 6 - 13 Bit 0.5 -10 kS/s 10µW Analog-Frontend

## Key Parameters

- Resolution: 6 - 13 bit
- Input bandwidth: 31 kHz
- ENOB: 12.6 bit
- Power consumption: 10.5 µW @ 1kHz
- Supply voltage: 1.8 V
- Operation clock: 140 kHz
- Differential input: +-1.7 V
- Programable Gain: -6 up to 12 dB
- Silicon area: 0.16 $mm^2$

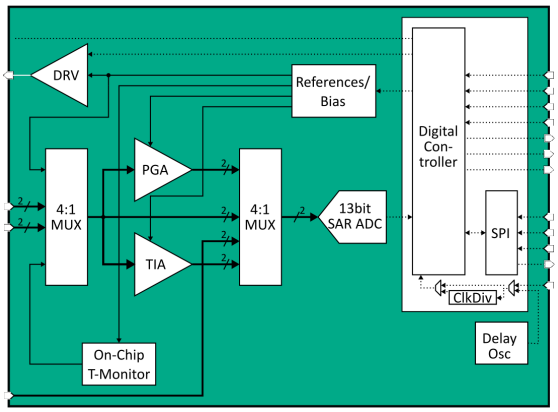


Fig. 1: IP-Level Block Diagram

## General Description

The Analog-Frontend (AFE) IP consists of programmable current and voltage preamplifier followed by a Successive Approximation Register (SAR) architecture ADC using charge-redistribution technique. The ADC IP is configurable regarding resolution (6-13 bit) and sample rate (up to 10kS/s). The preamplifier offers programmable gain from 0.5 to 4. The input voltage range is quasi-rail-to-rail guaranteeing more than +-1.7 V @ 1.8V power supply. An optional calibration technique can be applied to compensate degraded mismatch behavior of technology capacitors. The overall power consumption of the AFE IP sums up with 10.5 µW at 1 kHz input signal.

The AFE ASIC with current and voltage input channels was applied to commercial environmental sensors for ambient light, temperature and CO gas. An internal temperature monitor is included.

The AFE ASIC as well as the stand-alone SAR ADC are **silicon evaluated** using the **XFAB XT018** process. Measurement results and samples are available. The AFE IP was migrated to GF 22FDX.

Fraunhofer IIS/EAS provides a **detailed documentation** and **support** for the IP integration. **Modifications, extensions and technology ports** of the IP are available on request.

## Reference

Jotschke et al., A 10.5 µW programmable SAR ADC Frontend with SC Preamplifier for Low-Power IoT Sensor Nodes: IEEE 6th Virtual World Forum on Internet of Things, WF-IoT 2020.

## Benefits

- Low design risk due to silicon evaluated design
- Easy to use input due to integrated input buffer
- Selectable power consumption due to integrated automatic power-down function
- Task dependent selectable resolution
- Flexible use due to single-conversion and continous-conversion mode

## Deliverables

- GDSII data
- Simulation model
- Documentation
- Silicon validation report
- Integration support

FACT SHEET

**CONTACT**

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