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DATASHEET
RF FRONT END FOR LPWAN BASE STATIONS

Figure 1.
RF Front End PCIe Card with SMA RF Connectors

This Fraunhofer RF front end is a bidirectional, high dynamic range software defined radio (SDR) front end for Low-power wide-area networks (LPWANs) base station applications.

The RF front end supports up to three frequency bands with an instantaneous bandwidth of 2 MHz. The receiver is based on a super-heterodyne architecture with a 16 Bit IF sampling ADC for low noise and high linearity. The transmitter supports output powers of up to 500 mW (27 dBm). A standard PCIe interface (alternatively USB 3.0) is used for baseband (IQ) data, control information and firmware update. The PCB is a half-length PCIe card which easily integrates into a host PC. A host software provides access to the front end via the well-documented Fraunhofer IIS transceiver API. This allows an easy implementation of customer specific applications.

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Key Performance Parameters

The RF front end supports three frequency bands, which are configured for SRD860, ISM915 and LPD433 operation. The instantaneous bandwidth is 2 MHz and the baseband (IQ) sample rate is 2.4375 MSps.

The RF interface is composed of 50 ohms SMA connectors. A 10 MHz external reference input and a PPS input are available. The RF front end PCB measures 107 x 175 mm.

Table 1 sums up the key performance parameters of receiver and transmitter:

Parameters	**868 MHz**	**916 MHz**	**433 MHz**
Receiver (measured at nominal gain)			
NF	<4.5 dB	<4.5 dB	<4.0 dB
IIP3 (out of band)	>40 dBm (at LTE20)	>40 dBm (at 900 MHz)	>40 dBm (at 460 MHz)
IIP3 (inband)	>-15 dBm	>-15 dBm	>-20 dBm
Transmitter			
Pout (max.)	27 dBm	27 dBm	10 dBm

Table 1.
RF Front End Key Performance Parameters

Layout of Hard-, Firm- and Software

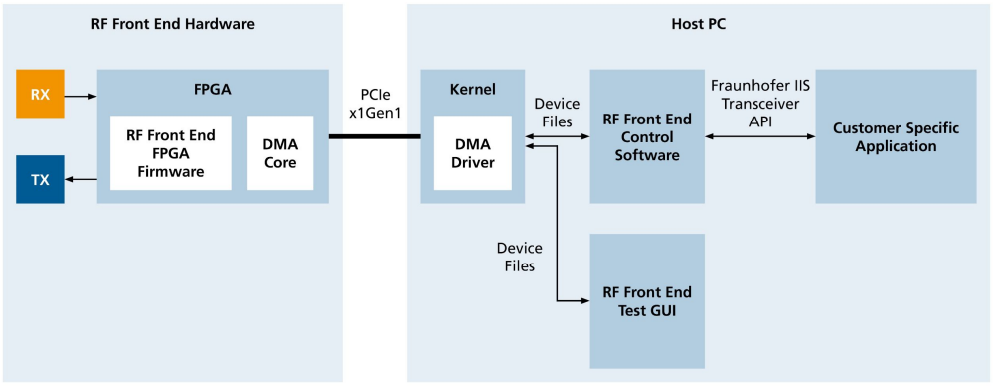

Figure 2.
RF Front End Architecture

Figure 2 depicts the following two building blocks of the RF front end:

- RF front end hardware, which contains receive and transmission chains as well as an FPGA running the RF front end firmware.
- Linux or Windows host PC running either the RF front end control software, which provides access to the transceiver API, or the RF front end evaluation GUI for testing.

The RF front end hardware and host PC are connected via PCIe x1 Gen1 and the data transfer is managed by the commercially available Xillybus IP core and kernel driver.