Fraunhofer IIS

WHITE PAPER

CORE DESIGN KITS

REFERENCE AND TEMPLATE CODE FOR MPEG AUDIO ENCODERS AND DECODERS ON EMBEDDED AND DIGITAL SIGNAL PROCESSORS

Fraunhofer IIS Core Design Kits (CDKs) are bit precise reference codes tailored for implementations of MPEG audio codecs on embedded and digital signal processors. They are optimized for devices with low resources in terms of memory and computational power. Currently, several MPEG Layer-3 and MPEG AAC encoders and decoders are available.

Fraunhofer Institute for
Integrated Circuits IIS

Director
Prof. Dr.-Ing. Albert Heuberger
Am Wolfsmantel 33
91058 Erlangen
www.iis.fraunhofer.de

Contact
Matthias Rose
Phone +49 9131 776-6175
matthias.rose@iis.fraunhofer.de

Contact USA
Fraunhofer USA, Inc.
Digital Media Technologies*
Phone +1 408 573 9900
codecs@dmt.fraunhofer.org

Contact China
Toni Fiedler
Phone +86 138 1165 4675
china@iis.fraunhofer.de

* Fraunhofer USA Digital Media Technologies, a division of Fraunhofer USA, Inc., promotes and supports the products of Fraunhofer IIS in the U. S.

OBJECTIVE OF THE CDKS

A DSP or embedded implementation of an MPEG audio coding algorithm requires a reference code. Usually this reference is derived from the algorithm development phase, i.e. it is written in floating point code. As the main focus is on flexibility, a floating point reference is usually not optimized for minimum requirements. The traditional approach to implement a reference code on a DSP or an embedded device is to go directly from the reference to the final implementation which is a time consuming process due to the algorithmic sophistication of modern audio codecs and the significant amount of floating point arithmetic used.
In contrast to this, the Fraunhofer IIS CDKs already include all fixed point specific know-how and optimizations and have been tested for stability and quality. The transition from the CDK to the final implementation can be done with less effort by simply adding processor specific optimizations such as assembler subroutines or support for Harvard architecture (see Figure 1), if this is necessary at all.
The Fraunhofer IIS CDK is a bit precise fixed point reference. Besides the bit true model, the CDK is optimized for memory requirements and processing power. The CDKs are written in C or C++ and are available in two different versions. One version is directly compilable for 16-bit or 32-bit integer RISC processors or DSPs, the other version is a template code for DSPs with fractional or integer arithmetic of any word length.

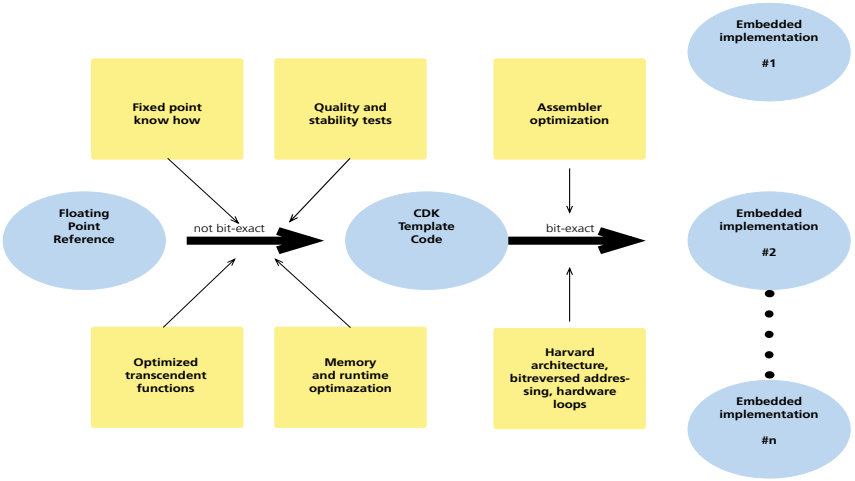

Figure 1: Development flow using the Core Design Kit template code.

16/32-BIT RISC PROCESSORS, CORES, AND DSPS

Special versions of the MPEG Layer-3 and MPEG AAC codecs are available for 32-bit processors and cores with integer arithmetic. These CDKs can be compiled directly for the target platform and are written in C++ or C. Assembler optimizations are available for several common 16/32-bit cores and compilers. An implementation on 16-bit devices is possible with the use of double precision arithmetic.
The CDK templates have been implemented on various ARM, MIPS32, embedded PowerPC, Analog Devices Blackfin and Texas Instruments TMS320C6x (DaVinci, OMAP) and

other processors. Appropriate project files and makefiles as well as example frame programs are available for various compiler tool sets.

DSP IMPLEMENTATION TEMPLATES

The arithmetic behavior of the target processor is encapsulated in a C++ library. This simulation covers data width of both, accumulators and memory location, fractional arithmetic, rounding, saturation, etc. As a consequence, the arithmetic library in the template code has to be adapted to the target device. In the final implementation, all C++ parts can be omitted since this behavior is present in hardware in the arithmetic logic unit of the processor.

This version of the CDK is basically not meant to be directly compiled for a target platform, although it could if there is an appropriate compiler available. It mostly acts as a template for an implementation in assembler. The advantage in comparison to a floating point reference is the fact, that the CDK already includes all fixed point specific items. Among others, these are scaling, transcendent functions etc. The correct behavior of the port can be easily verified after each processing stage by bit precise comparison to the template code.

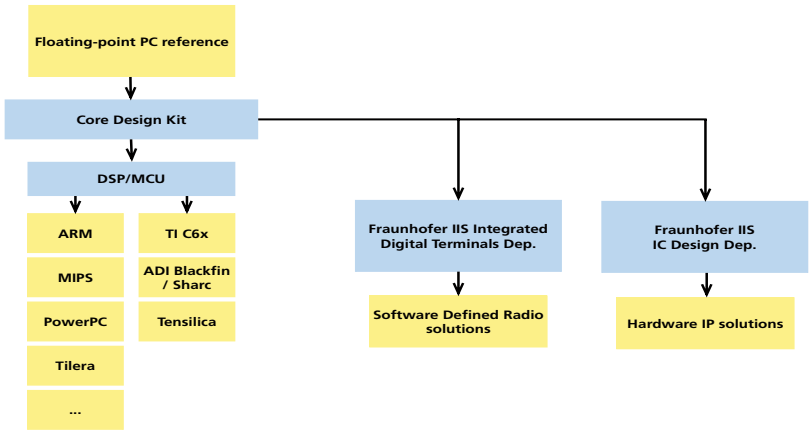

Figure 2: The Core Design Kit and a selection of processor types and cores for which it is suitable.

TARGET DEVICES

Due to their DSP-specific architecture, the main focus for the CDKs have been digital signal processors with fractional arithmetic. Today, the border between DSPs and micro controllers vanishes towards an integrated approach. Many of the currently available micro controllers with integer arithmetic supply sufficient computational power to do at least MPEG audio decoding.
The native data width may vary between 16 bits and 32 bits. In case of 16-bit devices, some parts of the algorithm have to be executed in 32-bit precision mode. Hardware support for double precision arithmetic on such devices might help to reduce the additional amount of processing power.
Figure 2 shows the different versions of the CDK which are available and gives examples of processor types and cores for which these CDKs are suitable, of course without being complete here.

REQUIREMENTS ON 16/32-BIT RISC PROCESSORS AND DIGITAL SIGNAL PROCESSORS

Requirement specification for the 16/32-bit RISC versions and also for the 20-bit or 24-bit DSP versions of MPEG Layer-3, MPEG-4 AAC-LC (AOT 2), MPEG-4 HE-AAC v2 (High Efficiency AAC), and MPEG-4 AAC Low Delay (AOT 23) codecs can be found in table 1. All values specify stereo signals at up to 48 KHz audio sampling frequency. These versions are optimized for low processing power and preferably use tables instead of computation where possible. They do not use special memory compression techniques like packed tables which would increase the required processing power.
The right-most column in Table 1 gives an example of practical, "real-life" processing power requirements of implementations of the CDKs on a 32-bit RISC processor. Actual processing power consumption can vary significantly depending on available internal program and data memory or cache and other architectural benefits like for example a Harvard memory architecture. A DSP-specific instruction set and often a certain amount of assembler optimization is necessary to reach low processing power values.
Program code size can vary heavily depending on the target processor and is not included in table 1. As an example, the code size for an AAC-LC decoder on ARM9E is about 50 KB, while for an HE-AAC v2 decoder it is around 100 KB. This code size needs to be added to the data ROM figures in table 1.

Algorithm (Stereo)	Data RAM [KBytes]	Data ROM[1] [KBytes]	Power [MIPS] (example)	Power [MHz] (example)
MPEG Layer-3 (MP3) Decoder	30	20	20-35	<35
MPEG Layer-3 (MP3) Encoder	55	21	50-60	<100
MPEG-4 AAC-LC (AOT 2) Decoder	20	18	20-30	<30
MPEG-4 AAC-LC (AOT 2) Encoder	60	20	30-70	<70
MPEG-4 HE-AAC Decoder (incl. SBR)	40	23	30-50	<50
MPEG-4 HE-AAC Encoder (incl. SBR)	105	38	60-110	<110
MPEG-4 HE-AAC v2 Decoder (incl. SBR + PS)	59	32	40-70	<80
MPEG-4 HE-AAC v2 Encoder (incl. SBR + PS)	160	40	80-110	<110
MPEG-4 AAC Low Delay (AOT 23) Decoder	18	17	25-30	<40
MPEG-4 AAC Low Delay (AOT 23) Encoder	50	13	70-80	<80

Table 1: Requirement specification for 2-channel stereo MPEG Layer-3, MPEG-4 AAC-LC (AOT 2), MPEG-4 HE-AAC (High Efficiency AAC), and MPEG-4 AAC Low Delay (AOT 23) codecs on 16/32-bit RISC processors.

Algorithm (5.1 multichannel)	Data RAM [KBytes]	Data ROM[1] [KBytes]	Power [MIPS] (example)	Power [MHz] (example)
MPEG-4 AAC-LC (AOT 2) Decoder	77	18	60-80	<80
MPEG-4 HE-AAC Decoder (incl. SBR)	130	33	80-130	<130

Table 2: Requirement specification for 5.1 channel MPEG-4 AAC-LC (AOT 2) and MPEG-4 HE-AAC (High Efficiency AAC) codecs on 16/32-bit RISC processors.

[1]Data ROM requirements are valid for frame length 1024 or 960 in the case of MPEG-4 AAC-LC and for frame length 512 or 480 in the case of MPEG-4 AAC Low Delay. Data ROM requirements are higher if more than one frame length needs to be supported. Data ROM does not include program code.

INPUT AND OUTPUT BUFFER REQUIREMENTS

In addition to the data RAM requirements stated above a certain amount of memory needs to be reserved for audio and bitstream input and output buffers. A decoder requires bitstream input and audio output buffers, an encoder requires audio input buffers and bitstream output buffers.
Depending on the type of application or environment in which the codec should run some of these buffers may need to be double buffers. For example in an encoder real-time environment where audio is continuously written into the input buffer (e.g. at 44.1 KHz sampling frequency) one part of the buffer needs to be save from being overwritten while the encoder is doing calculations on these values. The same is true for the encoder's bitstream output buffer if bitstream is written out at a constant bitrate and not in bursts. These considerations also apply to the decoder's input and output buffers. The minimum buffer sizes can be used only if the buffers are written and emptied in one single burst like for example in a file-I/O application. Table 2 shows the minimum and double buffering input and output buffer requirements for MPEG audio codecs. Bitstream buffer sizes are in bits or Kbytes, PCM audio buffer sizes are in PCM words (usually 16-bit or more). All values are valid for stereo and need to be multiplied by an appropriate factor for example for 5.1 or 7.1 multi-channel.

Algorithm (Stereo)	Minimum bitstream buffer size	Bitstream buffer size (double buffering)	Minimum PCM audio buffer size (samples)	PCM audio buffer size (double buffering)
MPEG Layer-3 (MP3) Decoder	11520 bits	~ 3 KBytes	1152	2304
MPEG Layer-3 (MP3) Encoder	11520 bits	~ 3 KBytes	1440	2592
MPEG-4 AAC-LC (AOT 2) Decoder	12288 bits	~ 3 KBytes	2048	4096
MPEG-4 AAC-LC (AOT 2) Encoder	12288 bits	~ 3 KBytes	5248	7296
MPEG-4 HE-AAC Decoder (also HE-AAC v2)	12288 bits	~ 3 KBytes	4096	8192
MPEG-4 HE-AAC Encoder (also HE-AAC v2)	12288 bits	~ 3 KBytes	7202	11298
MPEG-4 AAC Low Delay (AOT 23) Decoder	12288 bits	~ 3 KBytes	960	1920
MPEG-4 AAC Low Delay (AOT 23) Encoder	12288 bits	~ 3 KBytes	960	1920

Table 3: Input and output buffer requirement specification for MPEG Layer-3, MPEG-4 AAC-LC (AOT 2), MPEG-4 HE-AAC (High Efficiency AAC), and MPEG-4 AAC Low Delay (AOT 23) codecs.

MONO CODECS AND LOW AUDIO SAMPLING RATES

For a mono-only implementation of the above mentioned MPEG audio codecs the required data RAM and processing power can be reduced to about 60% of the stereo requirements. Data ROM and program memory cannot be significantly reduced in this case.
The required processing power scales linearly with the audio input/output sampling rate. For example a stereo encoder using 110 MHz at 48 KHz input sampling rate will need only around 30 MHz for encoding mono at 22.05 KHz input sampling rate.

CAPABILITIES AND QUALITY

The decoder CDKs for MPEG Layer-3 and MPEG-4 AAC are capable of decoding all standard compliant bitstreams with all standardized configurations. The audio output has been tested for compliance against the output of reference decoders.
Decoder CDKs for multichannel MPEG-4 AAC and other MPEG-4 Audio Object Types (e.g. MPEG-4 Error Robust object types) are available on request.

The encoder CDKs for MPEG Layer-3 and MPEG-4 AAC are capable of generating standard compliant bitstreams for all encoder configurations with up to two audio input channels and up to 96 KHz audio input sampling frequency. The audio quality of the generated bitstreams is comparable to floating point implementations of the same encoding algorithm.
Encoder CDKs for multichannel MPEG-4 AAC and other MPEG-4 Audio Object Types (e.g. MPEG-4 Error Robust object types) are available on request.

LICENSEES

Licensees of the Fraunhofer IIS CDKs are among others ARM Ltd., Cisco, NXP, ST Microelectronics, Toshiba, Texas Instruments.
Visit the partners and alliances section of our website for more references:
www.iis.fraunhofer.de/audio

LICENSING

MPEG Layer-3:
Software and patent licensing of Fraunhofer MPEG Layer-3 software is handled by Technicolor Licensing.
Please visit www.mp3licensing.com for more information.

MPEG-2 and MPEG-4 AAC:
Software licensing of Fraunhofer MPEG-2 and MPEG-4 AAC software is handled by Fraunhofer IIS.
Please contact amm-info@iis.fraunhofer.de by e-mail for more information.
MPEG-2 and MPEG-4 Audio patent licensing is handled by Via Licensing Alliance.
Please visit www.via-la.com for more information.

Version 06-2013

ABOUT FRAUNHOFER IIS

When it comes to advanced audio technologies for the rapidly evolving media world, Fraunhofer IIS stands alone. For more than 25 years, digital audio technology has been the principle focus of the Audio and Multimedia division of Fraunhofer Institute for Integrated Circuits (IIS). From the creation of mp3 and the co-development of AAC to the future of audio entertainment for broadcast, Fraunhofer IIS brings innovations in sound to reality. Today, technologies such as Fraunhofer Cingo for virtual surround sound, Fraunhofer Symphoria for automotive 3D audio, AAC-ELD for telephone calls with CD-like audio quality, and Dialogue Enhancement that allows television viewers to adjust dialogue volume to suit their personal preferences are among the division's most compelling new developments.

Fraunhofer IIS technologies enable more than 7 billion devices worldwide. The audio codec software and application-specific customizations are licensed to more than 1,000 companies. The division's mp3 and AAC audio codecs are now ubiquitous in mobile multimedia systems.

Fraunhofer IIS is based in Erlangen, Germany and is an institute of Fraunhofer-Gesellschaft. With 23,000 employees worldwide, Fraunhofer-Gesellschaft is comprised of 67 institutes making it Europe's largest research organization.

For more information, contact Matthias Rose, matthias.rose@iis.fraunhofer.de, or visit www.iis.fraunhofer.de/audio.