Experimental BOC Tracking Hardware Platform

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BIOGRAPHY

Philipp Neumaier received his Dipl.-Ing. degree in Electrical Engineering from the University of Stuttgart, Germany in 2008. Since 2009 he works at the Fraunhofer Institute for Integrated Circuits IIS in the field of GNSS receiver development with the emphasis of the digital baseband design.

Fabio Garzia received his Master of Science degree in Electronic Engineering from the University of Bologna, Bologna, Italy in 2005. In 2006 he joined the team of Prof. Jari Nurmi at the Tampere University of Technology (TUT), Tampere, Finnland, where he carried out his doctoral studies. His main research topic was the development of a coarse-grain reconfigurable array for the acceleration of multimedia processing in System-on-Chips. In 2009 he received his PhD degree and he continued his job as senior researcher at the TUT. In 2011 he moved to Germany where he joined the Navigation team at Fraunhofer IIS, Nuremberg. Since then he is charge of the development of SoCs and specialized hardware modules for GNSS receivers. The hardware implementation spans from ASIC to FPGA solutions. He takes care also of the hardware interface for the software layer as well as the low-level software integration.

Philipp Sommer received his Dipl.-Inf. degree in Computer Science from the Friedrich-Alexander-University, Erlangen-Nuremberg, Germany in 2010. Since the same year he works at the Fraunhofer Institute for Integrated Circuits IIS in the field of GNSS receiver development. His main task is the development of embedded system software which includes the planning and realization of the architecture for GNSS applications.

Alexander Rügamer received his Dipl.-Ing. (FH) degree in Electrical Engineering from the University of Applied Sciences Würzburg-Schweinfurt, Germany in 2007. Since the same year he works at the Fraunhofer Institute for Integrated Circuits IIS in the field of GNSS receiver development. He was promoted to Senior Engineer in February 2012. Since April 2013 he is head of a research group dealing with secure GNSS receivers and receivers for special applications. His main research interests focus on GNSS multi-band reception, integrated circuits and immunity to interference.

Günter Rohmer received his Dipl.-Ing. degree in Electrical Engineering in 1988 and the PhD in 1995 from the University of Erlangen, Germany. Since 2001 he is head of a department at the Fraunhofer Institute for Integrated Circuits dealing with the development of components for satellite navigation receivers, indoor navigation and microwave localization systems.

Jan Wendel received the Dipl.-Ing. and Dr.-Ing. degrees in Electrical Engineering from the University of Karlsruhe in 1998 and 2003, respectively. From 2003 until 2006 he was an assistant professor at the University of Karlsruhe, where his research interests focused on integrated navigation systems and MAV flight control. Since 2006, he is private lecturer at the University of Karlsruhe. In 2006, Jan Wendel joined MBDA in Munich, where he was responsible for the design, implementation and test of target tracking filters for the Medium Extended Air Defense System (MEADS), and for the development of navigation algorithms for a tightly coupled GPS/INS system demonstrator. In 2009, he joined EADS Astrium GmbH in Munich, where he is involved in various activities related to satellite navigation including acquisition and tracking algorithms, compatibility analysis, interference detection and characterisation, and EGNOS V3 NLES long loop control algorithms design.

Frank Max Schubert graduated in 2007 in Electrical Engineering and Information Technology at the Universitt Karlsruhe, today's Karlsruhe Institute of Technology in Germany. From 2007 until 2011 he was member of the scientific staff at the Institute of Communications and Navigation of the German Aerospace Center (DLR). He worked partly in the Wave Propagation and Interaction Section at the European Space Agency (ESA) in Noordwijk, The Netherlands, within the Networking/Partnering Initiative from 2008 until 2010. From 2009 until 2012 F. M. Schubert was an external Ph.D. student in the Navigation and Com-

munications Section at Aalborg University (AAU), Denmark. He obtained the Ph.D. degree from AAU in wireless communications in October 2012. Since November 2012 he is a system engineer for navigation signals at Airbus Defense and Space (formerly EADS Astrium) in Ottobrunn, Germany. His current activities comprise the research of DSP techniques for unambiguous tracking of high-rate BOC signals in real-life environments, the development of PRS receiver prototypes, and the data dissemination of the next generation of EGNOS.

ABSTRACT

Nearly all Global Navigation Satellite Systems (GNSS) use Binary Offset Carrier (BOC) for their current or modernized signals. Although BOC signals have many advantages over the legacy BPSK modulated ones, BOC tracking is more challenging due to its multiple peaks in the autocorrelation function. This paper describes a hardware architecture, its implementation, and first measurement results of an experimental software-assisted hardware receiver capable of providing measurements of different hardware correlator implementations in parallel in real-time. Three different correlator types will be described with emphasis on their hardware implementation efficiency especially selected for BOC tracking. The advantages of the special BOC tracking correlators - Double Estimator and Astrium Correlator - will be demonstrated in comparison to a standard early-prompt-late correlator. It is demonstrated that the hardware building blocks of the Standard Correlator can be reused for the sophisticated ones. Moreover, the FPGA area consumption of the sophisticated ones is not significantly higher than for the standard one.

INTRODUCTION

Galileo was the first GNSS to utilize BOC for its open service on E1 with BOC(1,1) and later updated to the modernized MBOC(6,1,1/11). Also the very wideband Galileo E5 AltBOC(15,10) signal is an origin of the BOC family. For Galileo PRS, BOC signals with a cosine-phased subcarrier (BOCc) are used. With the GPS III satellites there will be an additional open service signal namely the TM-BOC on GPS L1 whereas the modernized military signals, M-Code, are BOC(10,5) modulated on L1 and L2. Finally also the Russian GLONASS and BeiDou system designers are evaluating the usage of BOC.

The reason for this trend is that the BOC modulation has several advantages over the legacy Binary Phase Shift Keying (BPSK) modulation. Firstly, with BOC more energy is shifted to the edges of the band leading to a better spectral separation from the legacy BPSK signals, often sharing the same carrier frequency. Secondly, the theoretical tracking performance in terms of the Cramér-Rao-Lower-Bound (CRLB) improves with more energy at the edges of the frequency band. Thirdly, BOC signals have an inherent higher robustness against interferer: it has a slightly higher spreading gain thanks to the BOC and still single BOC side-lobes can be processed independently of the overall signal in case one side lobe is jammed. And finally its multipath mitigation capability is better compared to a BPSK signal without a subcarrier, thanks to its very narrow main peak.

But BOC processing, especially BOCc signals, sets some challenges: the BOC cross correlation function (CCF) consists of multiple peaks. It is crucial to track the right one, otherwise errors of several tens of meters are possible. For the BOC(1,1) with its three CCF peaks, a simple bump-jumping algorithm is robust enough and the tracking can still be done with a standard early-prompt-late (EPL) correlator. But especially the BOCc signals, with e.g. 11 peaks on the CCF for Galileo E1A BOCc(15,2.5), need a more sophisticated approach for a robust, peak-unambiguous BOC tracking. While it is easily possible in a software receiver to place as many correlator points on the CCF as desired for a specific tracking algorithm to work, in a real time operation hardware correlation channel, this has to be implemented and be traded off in an efficient way.

Many techniques exists for tracking BOC signals. Unfortunately some methods are very demanding of the hardware resources or/and do not take advantage of the improved accuracy of a BOC signal compared to an equivalent BPSK modulated one. In the developed versatile receiver platform, the three correlator types, Standard Correlator, Double Estimator (DE) and Astrium Correlator exploit the full capacity of the accuracy of the BOC signal. The different correlator types are described and analyzed with respect to there performance and hardware consumption.

This paper provides: a recapitulation of the BOC modulation, the description of the architecture of an experimental software-assisted hardware receiver where this work was done on, a detailed view on the implementation of the three hardware correlators, and first measurement results.

SIGNAL AND SYSTEM MODEL OF THE BINARY OFFSET CARRIER MODULATION

Signal theory

The BOC signals were introduced by Betz [1]. A BOC modulated signal uses a square wave subcarrier. Its baseband signal can be modeled as

$$\begin{aligned} s(t) &= x(t) + n(t) \\ &= \frac{A}{\sqrt{2}} \cdot d(t) \cdot c(t-\tau_0) \cdot g(t-\tau_0) \cdot e^{j(2\pi(f_D+f_{IF})+\Phi)} \\ &\quad + n(t) \end{aligned} \tag{1}$$

where A is the received amplitude of the signal, d is the navigation data bit, c is the pseudo random noise (PRN) spreading sequence, g is the subcarrier signal, f_D, f_{IF} and Φ is the Doppler frequency, the intermediate frequency (IF)

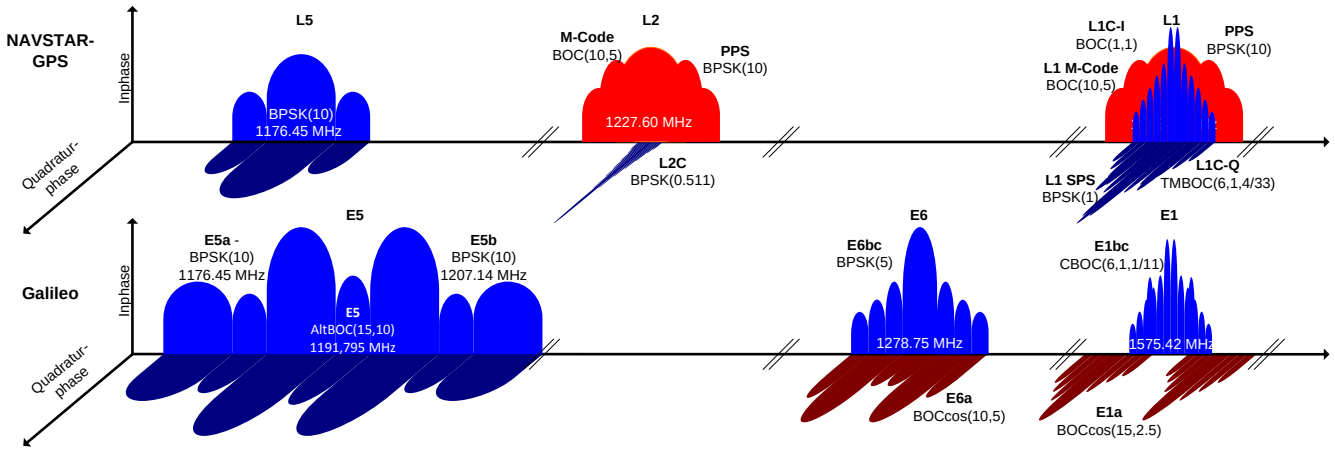
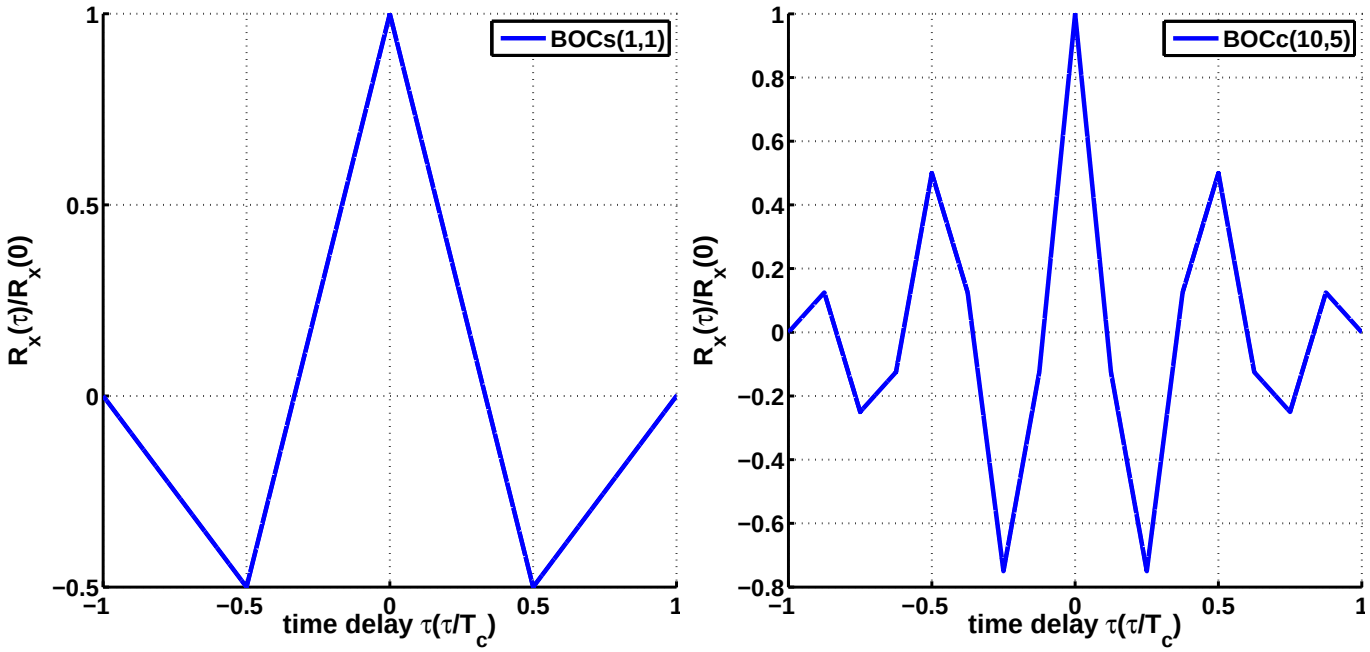


Figure 1. GPS and Galileo signals and their bands



(a) Galileo E1b/c BOCs(1,1) modulation

(b) Galileo E6a BOCc(10,5) modulation

Figure 2. Auto-correlation peaks of different BOCx(m,n) signals

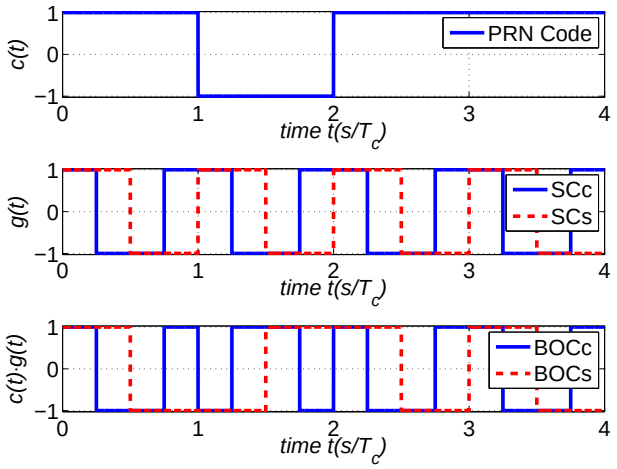


Figure 3. Part of a cosine-phased and a sine-phased BOC(1,1) code

and the initial phase, respectively and n is the noise component.

The waveform is denoted as BOCx(m,n), where the subcarrier frequency is defined to

$$f_{sc} = m \cdot 1.023\,\text{MHz} \tag{2}$$

and the PRN code rate to

$$f_c = n \cdot 1.023\,\text{MHz} \tag{3}$$

There are two types of BOC signals, one with a sine-phased subcarrier, described as

$$g_{sin}(t) = \text{sign}(\sin(2\pi f_{SC} t)) \tag{4}$$

and the other one with a cosine-phased subcarrier described with,

$$g_{cos}(t) = \text{sign}(\cos(2\pi f_{SC} t)). \tag{5}$$

The x is either "s" or "c" representing a sine-phased or a cosine-phased subcarrier, respectively. Figure 3 illustrates the resulting BOC signal in the time domain for sine and cosine subcarrier phasing. The main idea behind the BOC modulation is the shift of power form the center frequency to the edges of the band in order to increase the spectral separation with e.g. BPSK or BOCs(1,1) modulated signal sharing the same carrier frequency. The spectrum of BOC is split into two symmetrical parts around the carrier frequency, as depicted in Figure 4(b).

The autocorrelation function (ACF) of a BOC signal has has one primary peak and a certain number of secondary peaks. The number of secondary peaks depends on the subcarrier code frequency ratio and can be calculated with [2]:

$$n_{Peak} = \begin{cases} 4\frac{m}{n} - 2, & \text{BOCs} \\ 4\frac{m}{n}, & \text{BOCc} \end{cases} \tag{6}$$

A standard early-prompt-late (EPL) correlator in combination with a simple bump jumping (BJ) algorithm can reliably track the primary peak of a BOCs(1,1) signal with its two secondary peaks (Figure 2(a)). But the design complexity increases with an increasing number of secondary peaks. On the one hand the primary peak is much narrower than the peak of an corresponding BPSK signal. Hence the tracking accuracy rises due to less code jitter and higher multipath robustness. On the other hand the risk of the tracking loop to lock on an secondary peak increases. Due to filtering, noise, interference, multipath and dynamics a false lock is more likely to occur. As a result, undetectable side peak tracking resulting in systematic pseudorange errors: e.g. a false lock on the Galileo E6 BOCc(10,5) signal (its ACF is shown in Figure 2(b)) causes an error of around 15 m for each peak next to the primary one [3]. More sophisticated correlators than the EPL use structures to mitigate these false lock possibilities.

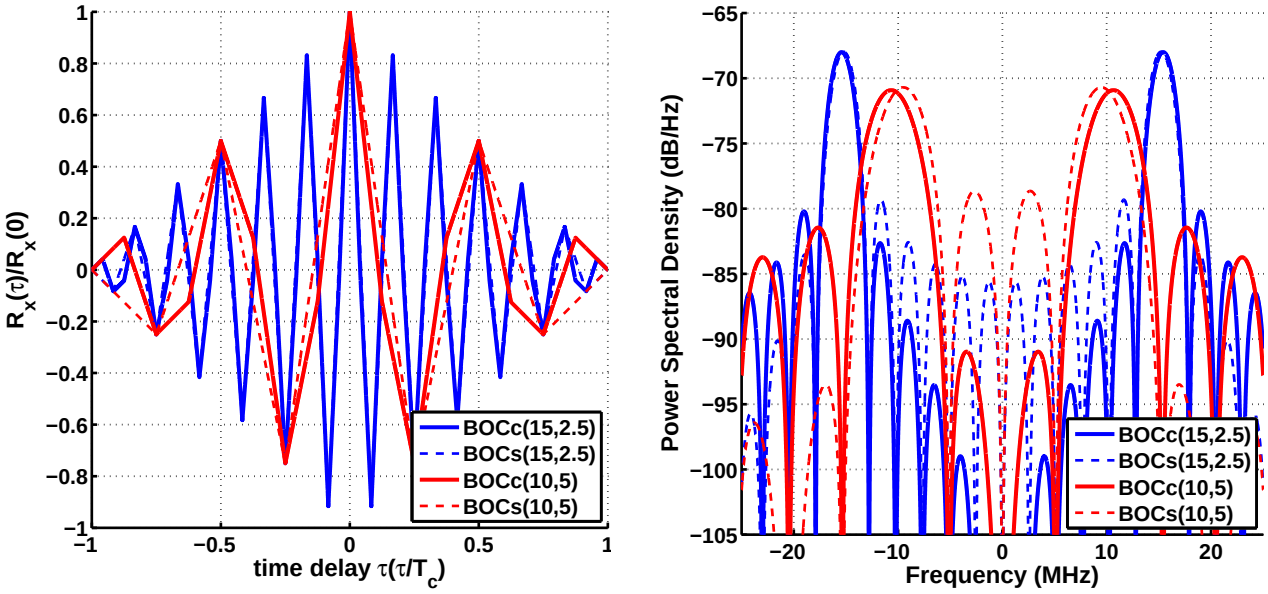
EXPERIMENTAL HARDWARE PLATFORM

Within the BaSE (Bavarian Security Receiver) project Fraunhofer IIS developed a versatile GNSS receiver platform capable of processing data from eight analog front-ends [4]. The receiver is intended as a two frequency, four element beamforming platform for the development and research of innovative Galileo PRS tracking and signal processing algorithms.

The block diagram of the BaSE baseband design is depicted in Figure 5. Eight multi gigabit transceivers (MGT) are used to receive the filtered and preprocessed digital data streams of the front-ends with a total data rate of 16.8 Gbit/s (4 channels E1, 4 channels E6 with MSPS75 at bit14 resolution in I/Q each). A 6-out-of-14 bit multiplexer allows to select the six effective bits to be used for the further baseband processing in the correlator hardware. At this stage, it is also possible to do a parallel snapshot of the raw front-end data to a so called covariance storage for the analysis of the different reception elements from the 2x2 beamforming antenna used.

The baseband hardware uses a dedicated fast Fourier transform (FFT) acquisition module to perform a parallel code phase search in the Fourier domain based on a 16 kSamples FFT. This enables a fast detection of the L1/E1 satellites with their respective code delays and Doppler frequencies. These Doppler results can have an accuracy of 2 Hz by using a pre-acquisition Doppler search step based on a novel patented algorithm [5]. This guarantees a faster and more reliable transition to the tracking.

The four E1 and E6 signals, respectively, can be assigned to any of the available tracking channels at run-time. This can be done in software by setting the value of a dedicated multiplexer. The basic system configuration consists of three different types of correlators - described in the following - with eight channels each. In the default assignment,



(a) ACF of various BOCx(m,n) signals

(b) Power spectral density

Figure 4. Comparison of a BOCx(15,2.5) and BOCx(10,5)

each antenna is connected to all three correlator types at the same time.

Using an application programming interface (API), the baseband FPGA can be controlled via a high-speed PCIe interface and the tracking loops closed in software on a standard Linux-PC. This approach uses the advantages of the fast parallel FPGA processing while still providing the flexibility of a software receiver.

There are two different baseband FPGA hardware designs: one experimental with three different types of correlators in parallel and one with 40 channels of the so called Astrium Correlators only as described in the following.

HARDWARE CORRELATOR MODULES

Different types of correlator structures with certain strength and weaknesses for BOC tracking are described in the literature. In the following, the three correlator types implemented in the BaSE experimental hardware receiver are described.

Standard Correlator

The Standard Correlator is a modified version of a conventional EPL tracking architecture (e.g [6]) with additional taps for very early (VE) and very late (VL) correlations. It contains two independent loops: a phase-locked loop (PLL) for carrier tracking and a delay-locked loop (DLL) for the code tracking. Both the Loops are independent and are controlled by numerically-controlled oscillator (NCO).

This correlator can track reliably low order BOC signals like a BOCs(1,1). To track higher order BOC signals some additional algorithms have to be used to ensure to track the main peak, e.g.:

Bump-Jump (BJ) The amplitude of the prompt correlator is compared to the amplitudes of two dedicated side peak correlators - very early (VE) and very late (VL) - having an offset of one subchip $\pm T_{sub}$ to intentionally place them on the side peaks. If an amplitude of one side peak correlator is higher than the prompt one, the tracking is in false lock and the prompt correlator "jumps" to the side peak correlator to get out of the false lock condition [7].

Auto Correlation Side-Peak Cancellation (ASPeCT) ASPeCT removes the side-peaks of an BOCs(n,n) signal by subtracting two squared correlation function: the CCF with its BOC replica and the CCF with its PRN replica only [8].

Multiple-Gate Discriminators (MGD) An unambiguous discriminator curve is synthesized by using a combination of multiple correlator taps. A vector of coefficients is used to weight the influence of each of correlation tap to shape an unambiguous BOC discriminator that has only one zero-crossing [9].

Single Sideband (SSB) The BOC sideband is separated by modulation and filtering in two separated BPSK signals. The correlation functions of the lower and upper sideband are added and the result is an unambiguous-BPSK like correlator peak [9].

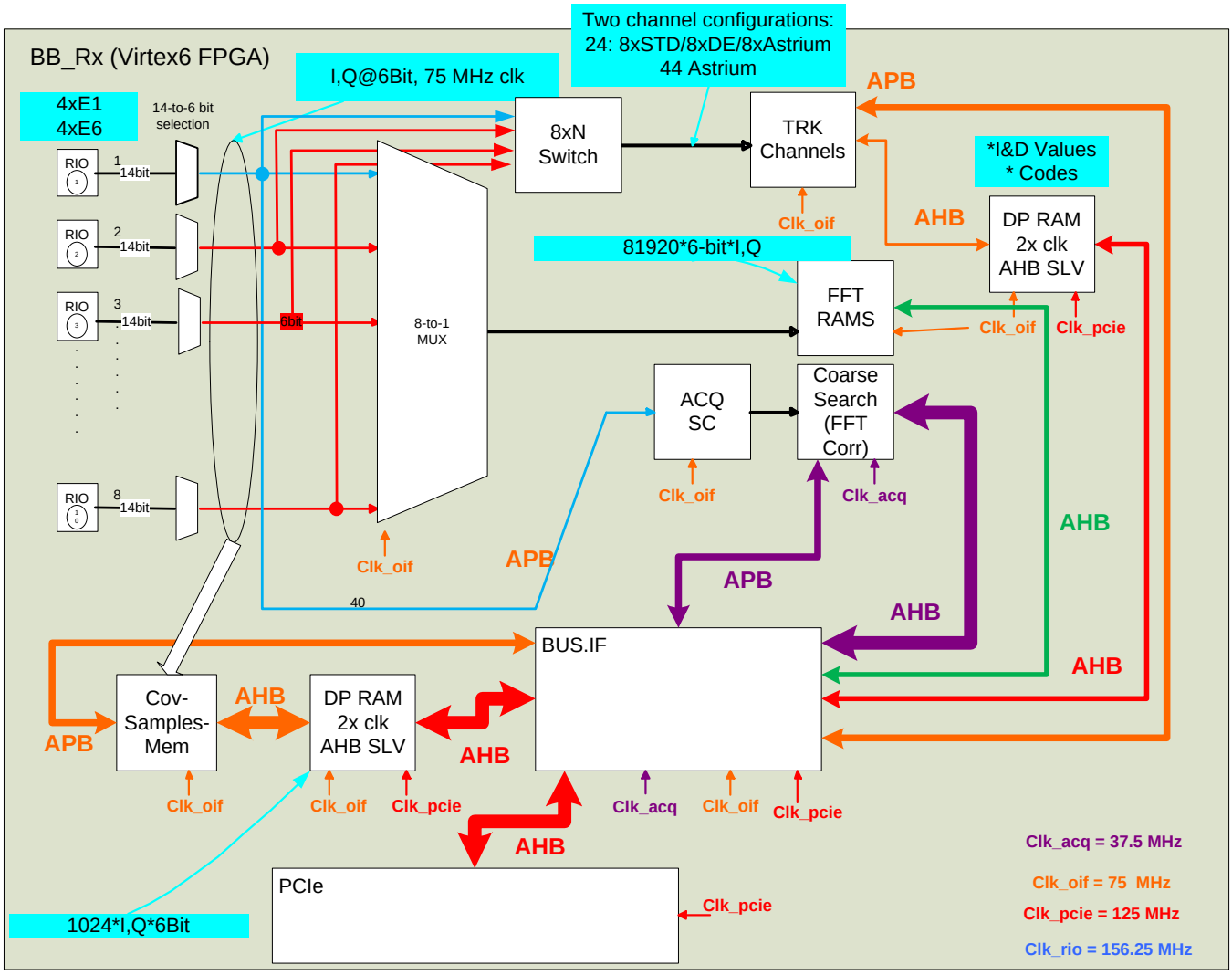


Figure 5. Baseband architecture block diagram of the experimental hardware platform

Double Estimator

The second correlator type is the Double Estimator (DE). In this module, the multiplication with code replica and signal is separated in three entities instead of two. Next to a standard PLL, the code phase will be simultaneously but independently tracked by a DLL and a subcarrier locked loop (SLL). The function space is now two dimensional for the sake of the independent code and subcarrier delay. This approach is a powerful technique to avoid the subcarrier ambiguities [10].

Astrium Correlator

The third correlator type implemented is the so called *Astrium Correlator* [3], [11]. The basic idea of the Astrium Correlator is similar to the DE but with only two loops: a PLL is used for carrier tracking and just one loop is used for coherent subcarrier and code tracking with five specific fixed subcarrier/code-relation replicas. As a result of the fixed alignment between subcarrier and code the SLL is sufficient in this case to still be able to track the BOC signals without peak ambiguity. The latter aspect is achieved by evaluating the result of the lock-to-false-peak detector of the Astrium Correlator.

IMPLEMENTATION EFFICIENCY

The three types of correlators are described in VHDL and implemented in parallel with eight channels each on a Xilinx Virtex 6 FPGA board - the so called baseband subsystem - next to a signal conditioning block, a hardware FFT acquisition engine and a PCIe-Interface for a PC. This baseband board is one core element of the BaSE receiver. The publication [12] provides a deeper look into the other hardware architecture details of the experimental BaSE Galileo PRS receiver.

Using an application programming interface (API) the baseband FPGA can be controlled via a high-speed PCIe interface and the tracking loops closed in software on a standard Linux-PC. This approach uses the advantages of the fast parallel FPGA processing while still providing the flexibility of a software receiver. A direct memory access (DMA) controller can transfer the NCO parameters and other data via DMA. This has the advantage that the CPU can simultaneously perform other tasks like tracking or PVT calculation. By using a PCIe connection the hardware does not suffer of a bottleneck by reason of the high data load between correlators and processor. Figure 5 illustrates the baseband architecture and shows the whole setup.

Standard Correlator

Using generics in the VHDL description for the input/output bit widths of the different modules, number of correlators and templates to select different components helps to find and verify the optimum setup for the desired application. Furthermore it provides distinct information about the size and performance of the hardware. Figure 6 shows the block diagram of the Standard Correlator. As explained before, the module consists of two independent tracking loops: the PLL or frequency-locked loop (FLL) to track the carrier and the DLL to track the PRN code. In addition to its classical implementation for BPSK signal with an early (E), prompt (P), and late (L) tap, there are implementation using an additional very early (VE) and verly late (VL) tap to be compliant with e.g. the BJ algorithm for BOCs(1,1) tracking.

There is a variety of literature where two additional time shifted replicas are used to mitigate multipath e.g. the high resolution correlator (HRC) [13]. The additional taps can as well be used to handle the multi peak ambiguity problem e.g. [14].

The not very complex, but computational demanding task of correlation is implemented in parallel in the FPGA hardware. The tracking loops are closed in the receiver software which is less computational demanding but more complex. The software program reads and writes hardware register in order to control the correlator.

The hardware implementation is presented in the block diagram 7. The correlator module consists of various small sub-blocks, which are described in the following:

A carrier NCO controls a quadrature mixer, for the sine and cosine wave generator in order to do the carrier wipe-off. The mixer can be implemented efficiently using a CORDIC algorithm or even more efficiently by a rectangular algorithm with just two output values -1, +1, resulting in an XOR operation for the mixer. For this platform both variations are implemented and can be selected by a generic.

The code tracking loop processor controls additionally the code NCO and with each overflow the correlator requests a new PRN chip. The chip is multiplied with the BOCx(1,1) subcarrier in the subcarrier generator submodule. This generator handles three states, the ordinary BPSK signal, the BOCs(1,1), and the BOCc(1,1) signal.

In this specific implementation, a code delay generator can generate up to 32 delayed replicas of a given PRN code. The spacing between the taps is adjustable during run time and can be controlled in the range of an 5 bit NCO. The replicas and incoming data samples (complex or real) are fed into an XOR gate based on the fact that the replica should contain values ± 1. After this step, these values are summed up in an accumulation register (integrated and dump). A small increment results in larger time to the overflow, which results in a smaller tap distribution over the correlation peak. The narrow-correlator techniques [15] uses this functionality. This feature is also necessary if the user wants to acquire different signals in one channel e.g. L1 and L5, where the chipping rate of the L5 signal is ten times higher. Figure 8(a) and 8(b) illustrate this result by using the same increment for the tap spacing for L1 and L5 in a

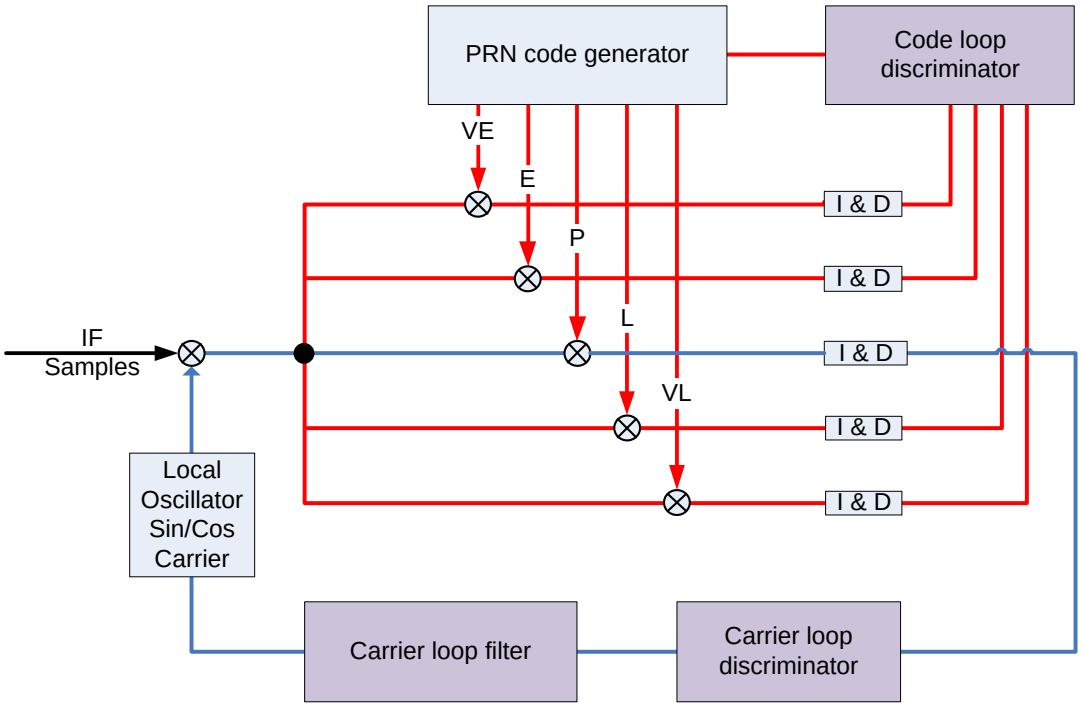


Figure 6. Structure of the Standard Correlator

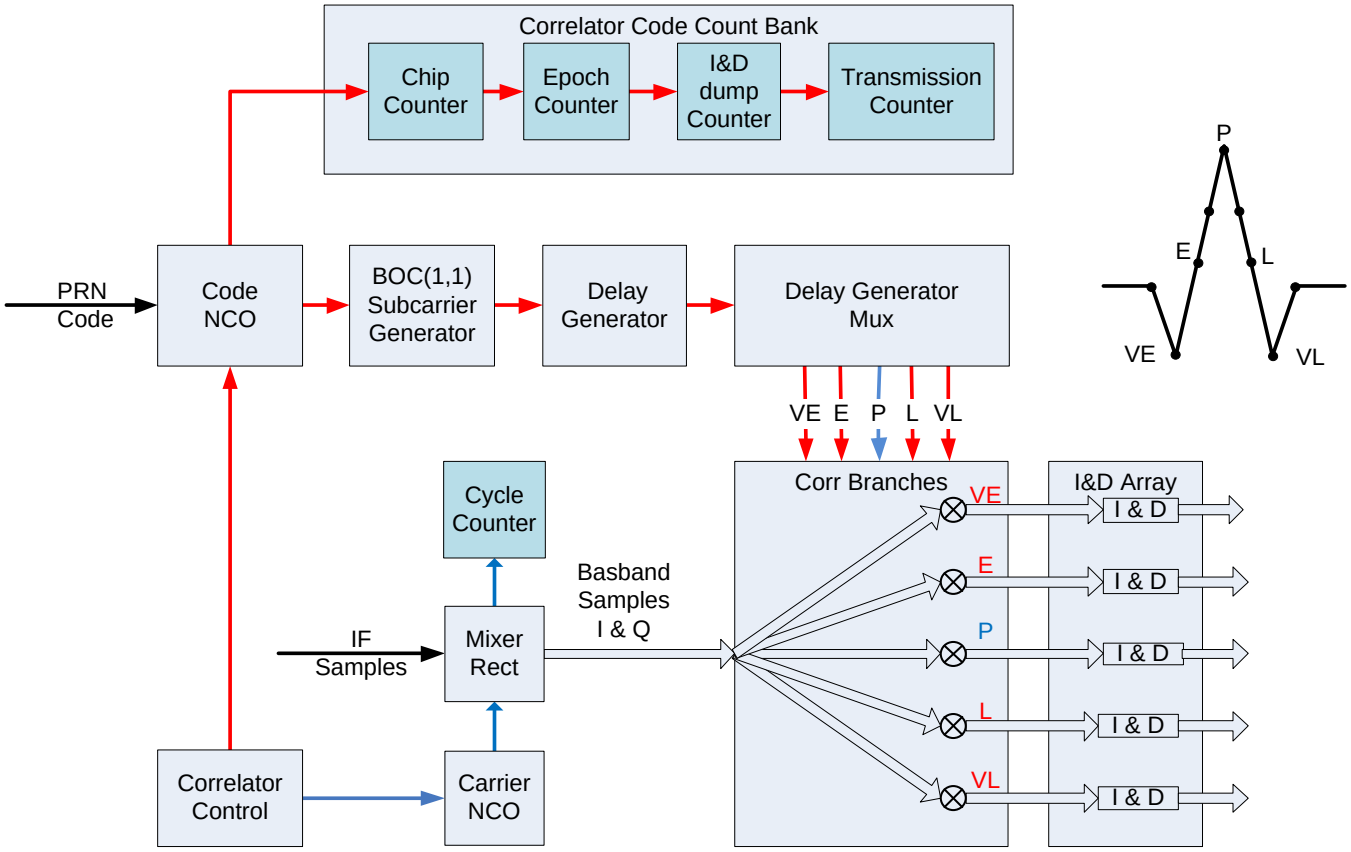
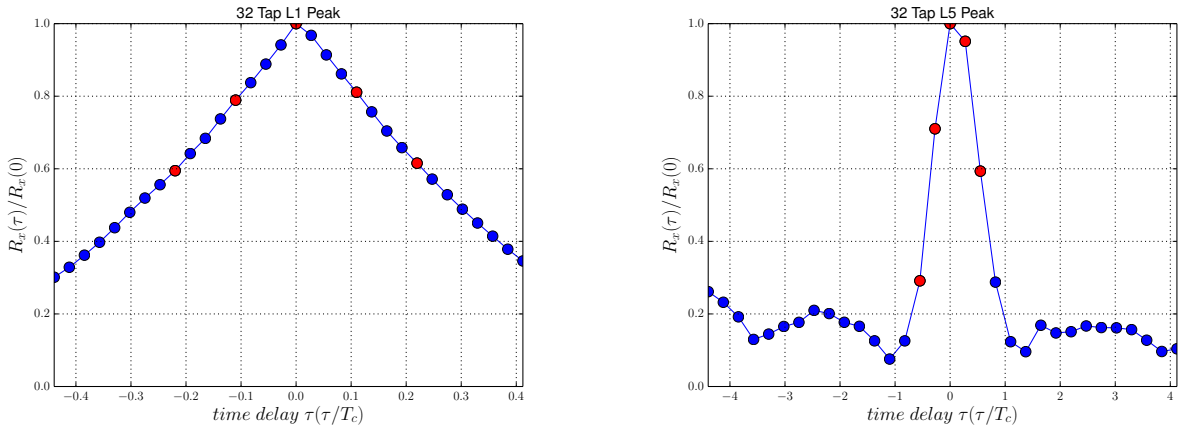


Figure 7. Block diagram of the Standard Correlator hardware implementation



(a) GPS L1 correlation peak with the increment of 16 for the correlator spacing

(b) GPS L5 correlation peak with the code increment of 16 for the correlator spacing

Figure 8. L1 and L5 correlation peak with the same spacing increment, $f_s = 75\,\text{MHz}$, open loop tracking

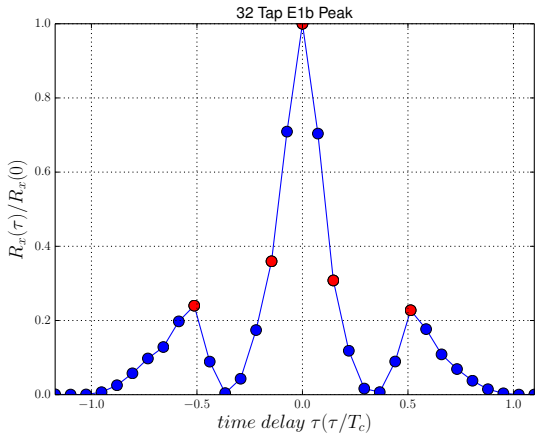


Figure 9. E1b 5 (red)- or 32 (blue) tap peak of a Standard Correlator, $f_s = 75\,\text{MHz}$, open loop tracking

32 multi-tap correlator. The use of 32 taps consumes a lot of hardware resources on the FPGA and the fact that the most tracking algorithm uses three or five taps only makes the concept of 32 taps dispensable. Therefore the correlator generates all 32 delayed replicas, but the software selects only five taps to calculate the Integrate and Dump (I&D) values. This selection is done in the *Delay Generator Mux* block, depending on the algorithm and signal modulation and can be changed during run time. Figure 9 shows an E1b correlation peak with all taps (blue) and an exemplary selection of five taps (red).

For developing new algorithm, for debugging purposes or further investigation in the correlation function e.g. harsh environment or multipath a 32 multi-tap correlator delivers some benefit. Maybe, in the future, there are new algorithm which need more correlator taps then five.

A common feature of new GNSS signals is the presence of two channels: data and pilot, that separately carry the navigation message and the data information. The data symbols in the signal limits the maximal coherent integration time, which can be set by the processor. Non-coherent integration is not supported by the hardware but can be done by the tracking software.

The output and the overflows of the NCOs feeds various counters, ridden by the processor during a defined time. With the output of the carrier NCO, the tracking software calculates the phase of the carrier. The code NCO output feeds the counter bank with the chip counter, epoch counter, I&D counter and transmission counter. This part is essential for an GNSS receiver because with these counter values the receiver calculates the pseudoranges. The counters are highlighted in turquoise in Figure 7.

Double Estimator

The Double Estimator solves the BOC signal's multiple correlation peak ambiguity problem by using a two dimensional correlation function. According to the block diagram in Figure 10 the DE has an additional independent loop, a SLL to control the generated replica of the subcarrier and to do subcarrier wipe-off. The increment of the subcarrier NCO provides an additional value for the pseudorange measurement. Due to the nature of the subcarrier, these result is an accurate and ambiguity phase τ_{SLL} compared with the code phase τ_{DLL} with less accuracy but no ambiguity.

$$\hat{\tau} = \tau_{SLL} + \text{round}(\frac{\tau_{DLL} - \tau_{SLL}}{T_{sc}/2}) \qquad (7)$$

Equation 7 describes the final delay estimate $\hat{\tau}$. Thanks to the rounding operation, the output is not affected if the code tracking error is smaller than half of a subcarrier chip.

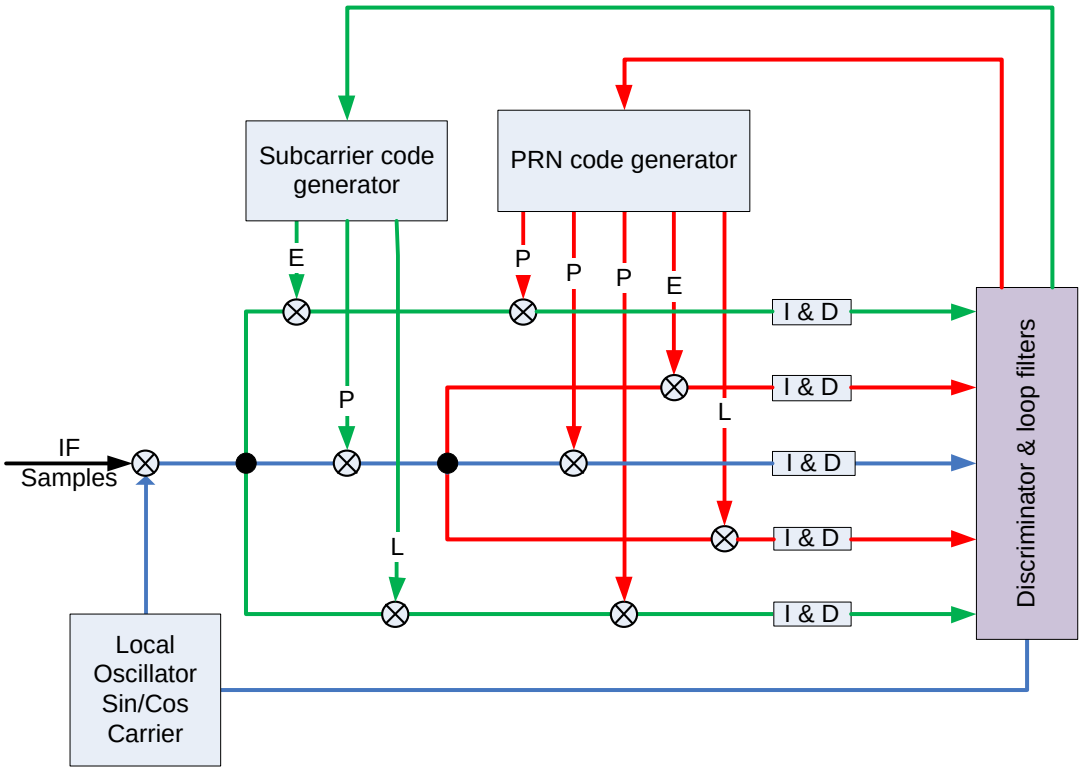


Figure 10. Structure of the Double Estimator

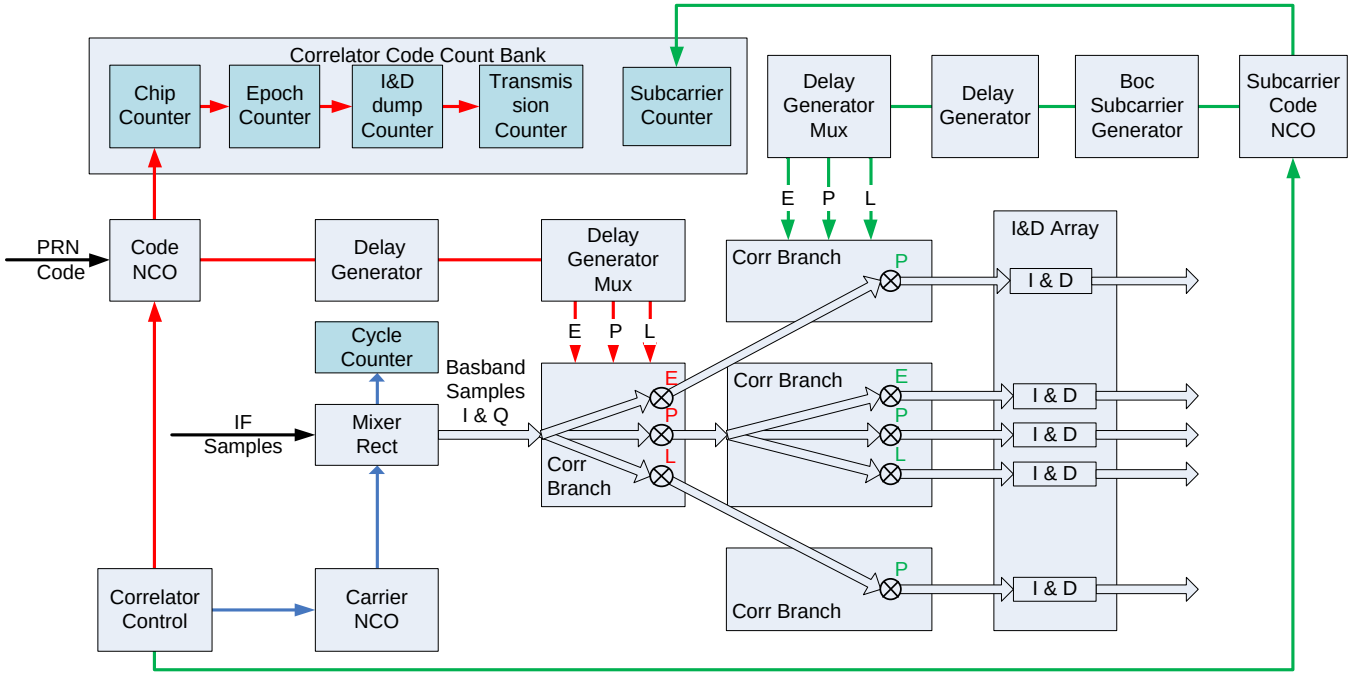


Figure 11. Block diagram of the Double Estimator hardware implementation

Figure 11 shows the implementation and the submodules of the DE architecture. In comparison with the earlier described Standard Correlator there are two independent operating delay generator block, two correlator branches and two Delay Generator MUX.

Astrium Correlator

Figure 12 shows the corresponding block diagram of the Astrium Correlator. In comparison with the DE it is important to distinguish that the architecture consist of only two loops. The first loop, the carrier loop is straight forward, it is equal to the architecture in Figure 6 and 10. In contrast to the DE, the second loop is a combination of code and subcarrier loop, controlled by only one NCO. The generated code and subcarrier are interlaced in the fallowing manner:

- Prompt subcarrier, prompt code (PP)
- Early subcarrier, prompt code (EP)
- Late subcarrier, prompt code (LP)
- Prompt subcarrier, early code (PE)
- Prompt subcarrier, late code (PL)

In comparison to the DE, the Astrium Correlator gets rid of an degree of freedom, of an independent subcarrier. This restriction is acceptable due to the fact that the satellite in an normal operation mode always transmits an aligned code and subcarrier.

Multiplying the input signal with the EP and LP replicas performs a code wipe-off. The result is used in an early-late discriminator to estimate the subcarrier tracking error. Multiplying the input signal with the PE and PL replicas performs a subcarrier wipe-off. The result is fed to a detector function:

$$D = PE^2 - PL^2 \tag{8}$$

If the tracking is locked on the main peak, the detector is zero-mean. In a false peak lock position, the mean of the detector significantly deviates from zero, and the sign shows weather the side peak lock occurs on the left or right from the main peak and can therefore be corrected. Figure 14 shows the detector function for a BOCc(10,5) signal.

This correlator type tracks BPSK signal as well, due the fact that the subcarrier can be set to one. E.g. Figure 15(a) shows the Astrium correlator with an L5 BPSK Signal and Figure 15(b) shows the E1b BOCs(1,1) signal, where the three inner points forms the main peak. The outer points are used for the detector function.

HARDWARE RESOURCES

The baseband hardware and its modules are described in VHDL and programmed to a FPGA (field programmable gate array), a scalable chip architecture based on pre-build blocks and programmable routing resources. The VHDL code is synthesized on an Xilinx Virtex6 XC6VLX240T FPGA using the Xilinx ISE 14.6i. The configurable logic blocks (CLBs) are the main logic resource and contain two slices connected to a switch matrix. Each slice contains four look-up tables (LUTs), eight storage elements (registers), wide-function multiplexers, and carry logic. Some slices support storing data using distributed RAM and shifting data with 32-bit registers [16].

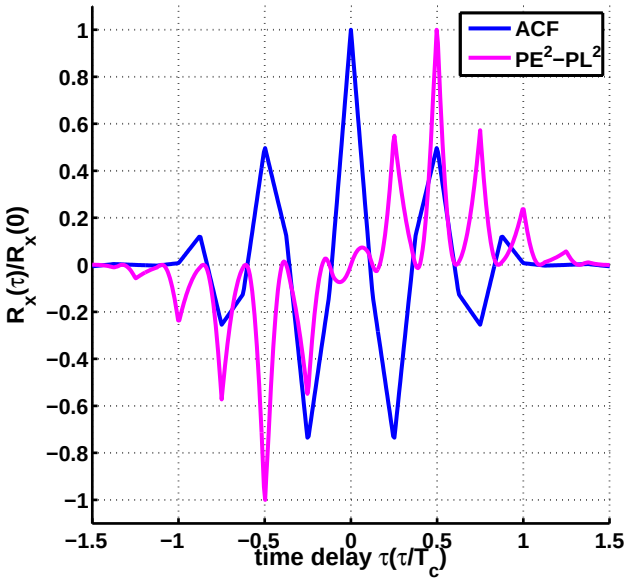


Figure 14. Blue plot shows ACF of a BOCc(10,5) signal and the Magenta plot shows the corresponding detector function

Table 1 summarizes the relevant information of the place and route (P&R) report. The first part of the table shows the hardware usage for each correlator type. As expected the hardware consumption increases slightly for the Astrium and DE correlator, respectively. The second part compares four different hardware implementation of the complete baseband receiver with 24 correlators each. The mixed baseband receiver has eight correlator of each type. By reason of the stochastic P&R algorithmic the results are almost equal and random. The mixed baseband receiver consumes the most resources probably as a result of higher complexity of three different types of correlators.

TEST AND RESULTS

Figure 17(a) and 17(b) demonstrate a BOC(1,1) signal tracking using the unambiguous Early-Minus-Late-Power discriminator (UEMLP) as described in [14]. Accordingly the Early-Late Spacing (ELS) and Very Early-Very Late Spacing is set to 0.5 chips and 0.5 chips, respectively.

Similarly, Figure 16 shows a L1 C/A BPSK signal tracking. The discriminator function corresponds to the well-known

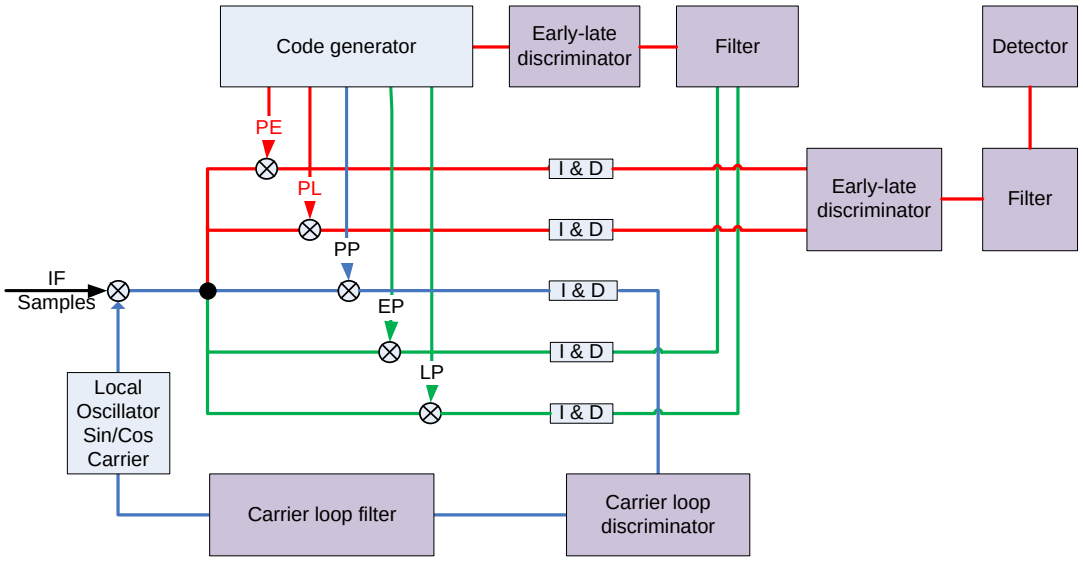


Figure 12. Structure of the Astrium Correlator

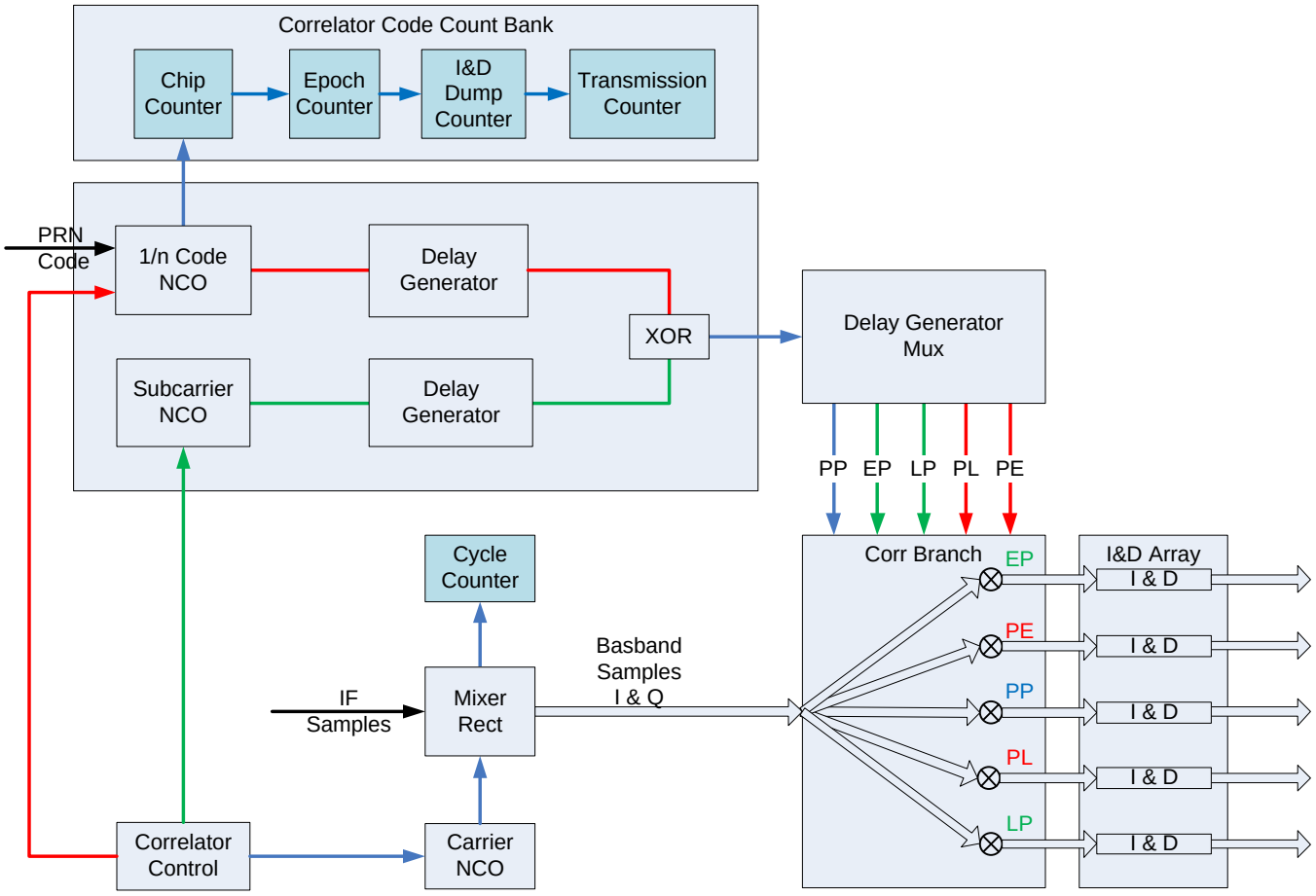
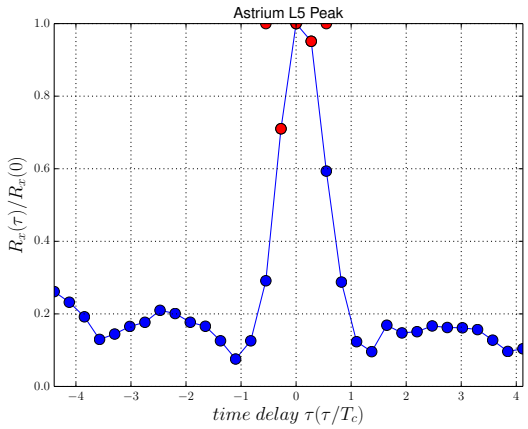
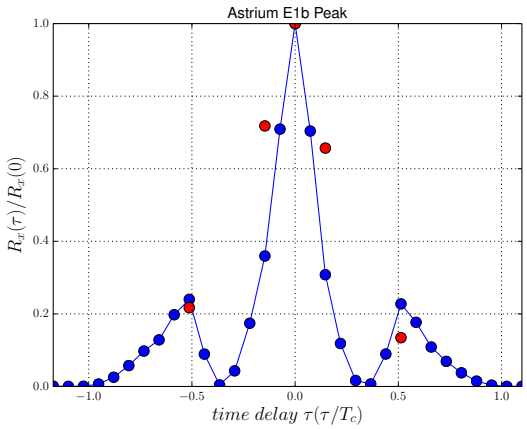


Figure 13. Block diagram of the Astrium Correlator hardware implementation



(a) Red plot shows the Astrium Correlator with P, E, P, L and P and the blue plot shows the 32 points-multi-tap correlator of the same signal

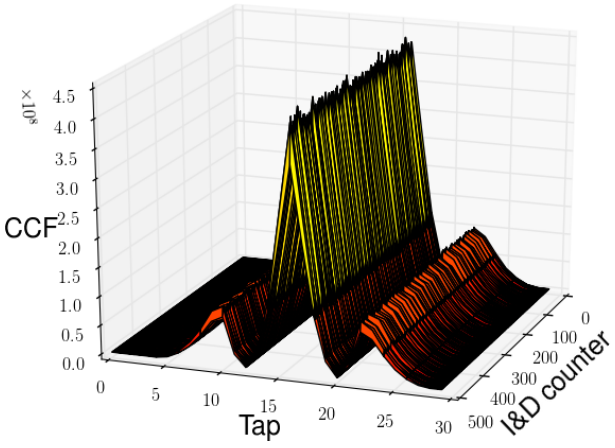


(b) Red plot shows the Astrium Correlator correlation peak with EP, PE, PP, PL and LP and the blue plot shows the 32 points-multi-tap correlation of the same signal

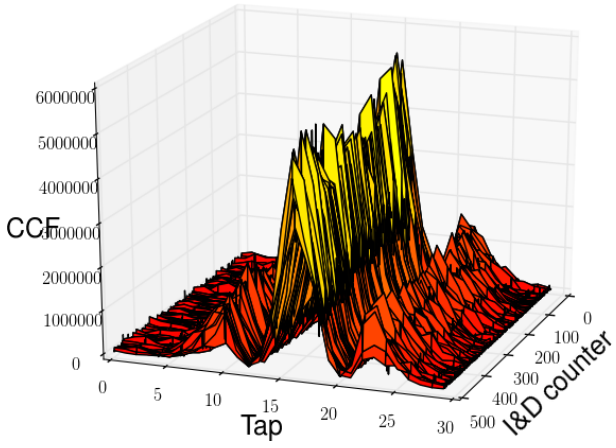
Figure 15. L5 and E1b signal, $f_s = 75\,\text{MHz}$

	Slices	Slice Registers	Slice LUTs	LUT RAM	Area
Correlator STD	751	2691	2790	24	1,99%
Correlator DE	824	2787	2827	24	2,19%
Correlator Astrium	979	2786	2829	24	2,60%
Receiver STD	29441	85533	92150	1120	78.13%
Receiver DE	29274	87887	93765	1120	77.69%
Receiver Astrium	30306	87865	93500	1120	80.43%
Receiver Mixed	30312	87861	94863	1120	80.45%

Table 1. P&R with Xilinx ISE 14.6i on a Virtex6 XC6VLX240T FPGA



(a) Synthetic signal without Gaussian noise



(b) Spirent signal generator

Figure 17. E1b BOC(1, 1) tracking with the integration time of 1 ms, 32 multi-tap correlator, $f_s = 25\,\text{MHz}$

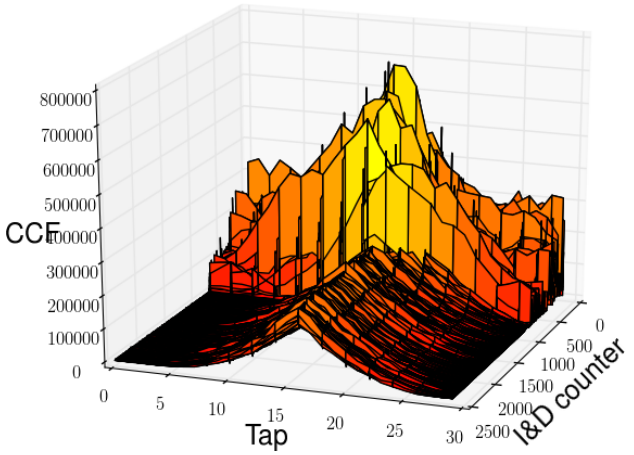


Figure 16. 32 tap L1 tracking with integration time of 1 ms and after 1000 ms switched to 20 ms coherent integration time

normalized Dot-Product discriminator also described in [14]. Here, a wide ELS of 0.5 chips is used. For the first 1000 I&D values, the integration time is 1 ms. After 1000 ms, the coherent integration time is 20 ms, therefore the I&D values are smoother. The absolute power is normalized.

CONCLUSION

In this paper a hardware platform with the emphasis for BOC Tracking was presented. It was shown that a modified version of EPL correlator brings some benefit for BOC(1,1) tracking. As well that 32-multi-peak correlator delivers some considerable advantages in the developing process of new algorithm. Also it was demonstrated that the implementation of the DE through a rearrangement and by adding some of the basic modules of the EPL correlator is straightforward. In addition the first implementation of a new correlator type the Astrium correlator which based as well on the EPL correlator and its standard modules. Furthermore the paper showed some of the measurement results of the closed-loop tracking process.

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