NAPA: A Fully Integrated Multi-constellation Two-frequency Single-chip GNSS Receiver

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***Abstract*—This paper presents the overall architecture, the implementation, test setup, and first measurements results of a fully integrated multi-constellation two-frequency single-chip GNSS receiver. The ASIC supports the simultaneous reception and processing of the GPS L1/L5, Galileo E1/E5a and GLONASS G1 signals with 40 versatile tracking channels. The dual-band analog RF front-end is integrated on the same mixed-signal chip as the baseband hardware including an embedded LEON2 processor to close the tracking loops. The chip was realized in a low-power 1.2 V 65 nm TSMC technology.**

***Index Terms*—Satellite navigation systems, Global Positioning System, Receiver, ASIC**

I. Introduction

Multi-constellation multi-band global navigation satellite system (GNSS) receivers can efficiently exploit the advantages deriving from the modernization of existing GNSS constellations such as GPS and GLONASS as well as from the launch of new ones like Galileo and BeiDou. In fact, the utilization of multiple systems can significantly improve the availability of a navigation solution in urban canyons and heavily-shadowed areas. In addition, the increased satellite availability guarantees higher measurement redundancy and improved reliability. Moreover, the excellent inherent noise and multipath mitigation capabilities of the new and modernized wideband signals in the L5/E5a band, combined with the ionosphere error mitigation given by frequency diversity, improves significantly the accuracy in both measurement and position domains [1].

Still most commercial fully integrated single-chip mass market GNSS receivers use only a single frequency band for their positioning, velocity, time (PVT) solution: namely GPS L1 C/A or in addition Galileo E1 and GLONASS G1. For example, the Teseo chips [2], [3] are single-chip solutions that supports multiple constellations but only on one frequency band. The main reason is to reduce the design costs and enable lowest power consumption. However, the advantages of wideband signal processing with the higher robustness of having two simultaneous frequency band receptions and the capability of mitigating the ionosphere error are neglected. Another approach to realize multi-constellation multi-frequency solutions is to combine different chips for the analog front-end and the digital baseband. In [4] a fully integrated single chip analog multi-band front-end for the simultaneous reception of GPS L1/L5, Galileo E1/E5 and GLONASS was presented. However, this chip included only the front-end and needs an additional, separate digital baseband solution. The purpose of the NAPA project (Navigationsempfänger Chipsatz für Personennavigation mit Anwendungen bei erhöhter Genauigkeit / **NA**vigation chip for **P**edestrian navigation and higher precision **A**pplications) is to close this gap by providing a fully integrated, compact, low-power, and low-cost solution where the analog and digital part of the GNSS receiver are integrated together on the same chip. The NAPA receiver offers all the advantages of multi-constellation reception with additional dual-frequency support.

The NAPA chip features a monolithic, single mixed-signal chip implementation of a multi-system, multi-band analog front-end and the related digital baseband core including an embedded processor. The NAPA chip can be used as a stand alone GNSS sensor, since no additional components are required to obtain a PVT solution. The ASIC was implemented in a low-power technology and adopts some ad-hoc low-power architectural features. From the cost point of view, an ASIC solution is more convenient than a FPGA one as long as the non-recurring engineering costs (NRE) are amortized by the amount of chips manufactured and sold.

The NAPA chip supports multi-system (GPS, Galileo and GLONASS) and multi-band (GPS/Galileo L1/E1, L5/E5a, GLONASS G1) processing. Figure 1 shows the frequency band being selected to be received and processed in the NAPA chip. With two fully deployed GNSS, GPS, and GLONASS, NAPA chip can already be used in many commercial applications. Thanks to the spectral overlay of the GPS L1/L5 and Galileo E1/E5a signals, the chip is also ready for Galileo. The frequency selection features both the narrow band legacy signals L1/G1 which can be used for fast acquisition. For highest tracking accuracy, the wideband GPS L5 and Galileo E5a BPSK(10) modulated signals can be utilized.

The higher accuracy is mainly obtained by the attenuation of the ionospheric error. The ionosphere is a dispersing media that can introduce a bias error between 1 and 20 m. Forming a linear combination of two independent frequency band measurements, the ionospheric bias can be measured and almost completely removed. In addition, Precise Point Positioning and

Wide/Narrow-laning combinations are possible thanks to the second received frequency band. The first allows to combine precise satellite positions and clocks with multi-frequency measurements providing cm/dm solutions. The second adopts fast ambiguity solutions for carrier-phase positioning and cycle-slip detection.

In this paper we present in detail the NAPA chip. The paper is organized as follows. First, we describe the architecture of the analog front-end and its digital counterpart with their innovative features. Then we provide details of the chip implementation, manufacturing and the test setup. Finally, we present first verification results before we draw the conclusion.

II. Architecture Overview

The NAPA architecture is depicted in Figure 3. It is composed of two separate blocks integrated on the same silicon die: the analog core provides the functionality of a two-frequency radio-frequency (RF) front-end whereas the digital part implements the main GNSS processing tasks, including the correlator channels and an embedded processor, and takes care of the RF front-end control. The interface between the two blocks is completely digital and provides synchronizers to ensure a valid clock domain crossing (CDC).

A. Analog Front-end

The analog RF front-end supports the simultaneous reception of GPS L5 / Galileo E5a and GPS L1 / Galileo E1 / GLONASS G1 signals as well as modes where only one reception path is activated.

Both passive and active GNSS antennas are supported thanks to integrated low noise amplifiers (LNA). There are two separate signal reception paths for the two frequency bands. The L1/E1/G1 path is characterized by a quasi-zero-IF conversion that mixes the middle frequency between L1/E1 and G1 to zero frequency. The L1/E1 reception bandwidth is up to 14 MHz, to incorporate also the MBOC modulations of Galileo E1 and future GPS L1C signals. A programmable automatic gain control (AGC) controls the complex analog baseband signals before they are digitized with a 4 bit dual channel analog digital converter (ADC).

The second reception path receives a L5/E5a signal with up to 20 MHz bandwidth for the BPSK(10) modulated signals. This path uses a low-IF architecture. The signal is down-converted to an intermediate frequency (IF) of 15.345 MHz. The image frequency is suppressed by a polyphase filter. The real-values analog signal is controlled by an AGC and converted to the digital domain using a single 4 bit ADC.

A common phase locked loop (PLL) is used with specific L1/E1/G1 and L5/E5a dividers to generate the mixers' local oscillator (LO) frequencies. The PLL loop filter is integrated on-chip to minimize external elements. Moreover, automatic filter and voltage controlled oscillator (VCO) calibrations are included to mitigate process tolerances. The PLL can handle input clock frequencies between 10-80 MHz with a recommended clock frequency of 36.115 MHz.

A SPI core was implemented on the front-end part to be able to control the different front-end features. E.g. it is possible to tune the PLL, to switch off a complete front-end path if the second frequency band is not used, and to active different on-chip calibration procedures.

The frequency plan of the front-end is depicted in Figure 2. Due to the quasi zero-IF architecture, the complex L1/E1 baseband signal is located on an IF of -13.64 MHz and the GLONASS G1 frequency division multiple access (FDMA) signals on an IF of +12.94 MHz with respect to the GLONASS G1 center frequency of 1602 MHz. The real valued L5/E5a signals are provided by the second ADC and located on an IF of 15.345 MHz.

The ADC samples are generated with a frequency of 74.4871875 MHz for both the single L5 as well as for the dual channel L1/E1/G1 ADCs. The ADC clock is also directly connected to the baseband digital core and is used as main clock for the GNSS hardware modules. The embedded processor in the digital core receives a second clock which is twice as fast as the GNSS hardware one.

B. Digital Baseband SoC

The baseband is characterized by a system-on-chip (SoC) architecture based on a SPARC compatible 32 bit LEON2 microprocessor [5] running at approx 150 MHz. The GNSS functionality including acquisition and tracking are implemented using dedicated hardware modules.

From a functional point of view, the processor is in charge of correctly configuring the RF-front-end and controlling the different parts of the receiver. In particular, it triggers the acquisition, it initializes and starts the tracking channels with the signals detected in the acquisition and takes care of closing the frequency/phase/delay locked loops (FLL/PLL/DLL) used for signal tracking. The tracking loops have strict real-time constraints, therefore the communication between the channels and the processor features a high-speed infrastructure.

From the structural point of view, the processor is connected to a hierarchical on-chip Advanced Microcontroller Bus Architecture (AMBA) composed of a high-performance bus (AHB) and a peripheral bus (APB). The AHB provides a direct connection between the processor, the real-time GNSS modules and the system memory, a monolithic 1 MByte block that hosts the main program at run-time. Different programs can be loaded if needed by using the external SD-card interface.

In addition to the processor, there are four additional AHB masters: the bootloader, the SD-card controller, the real-time GNSS modules and the on-chip processor debugger. The bootloader is in charge of the bus control at system start-up. The SD-card controller has integrated direct-memory access (DMA) capabilities to move data between the SD-card and the system memory. The real-time GNSS modules can write the tracking results directly to the system memory. Finally, the integrated processor debugger allows real-time debugging and is used mainly in the verification phase.

The APB provides a connection to generic peripherals, control and status interface of the GNSS modules without

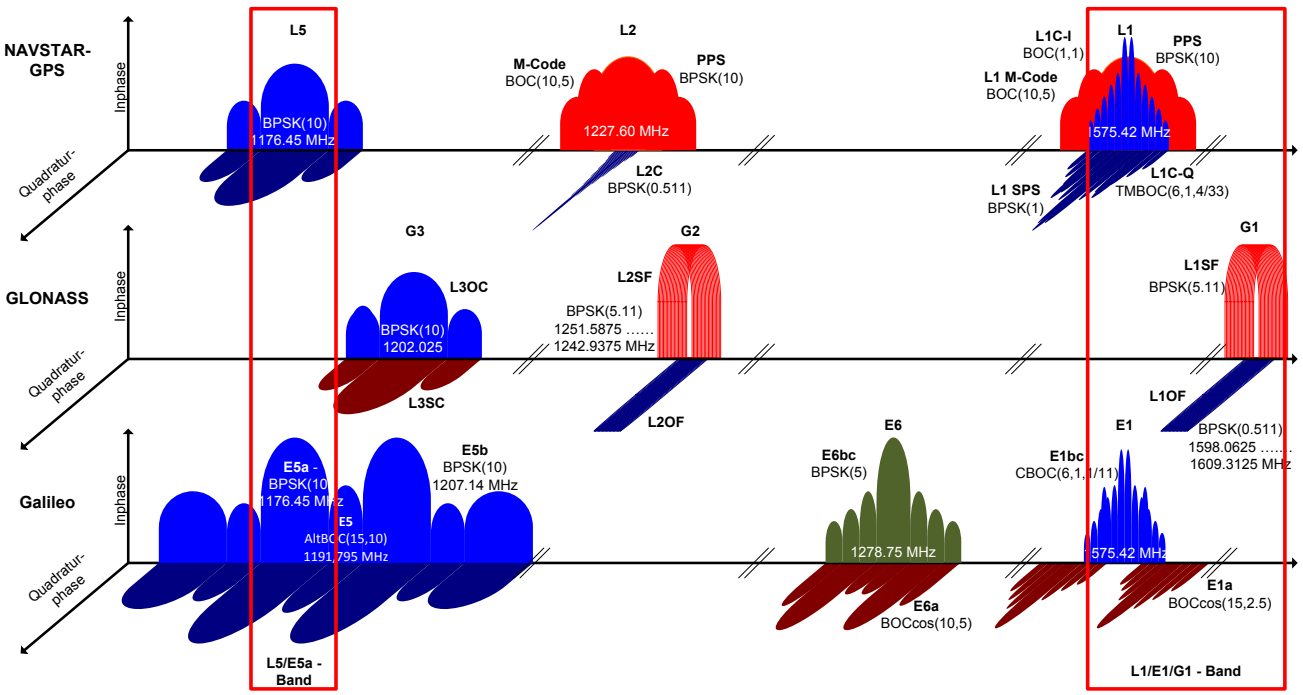

Figure 1. GNSS signals received and processed by the NAPA chip

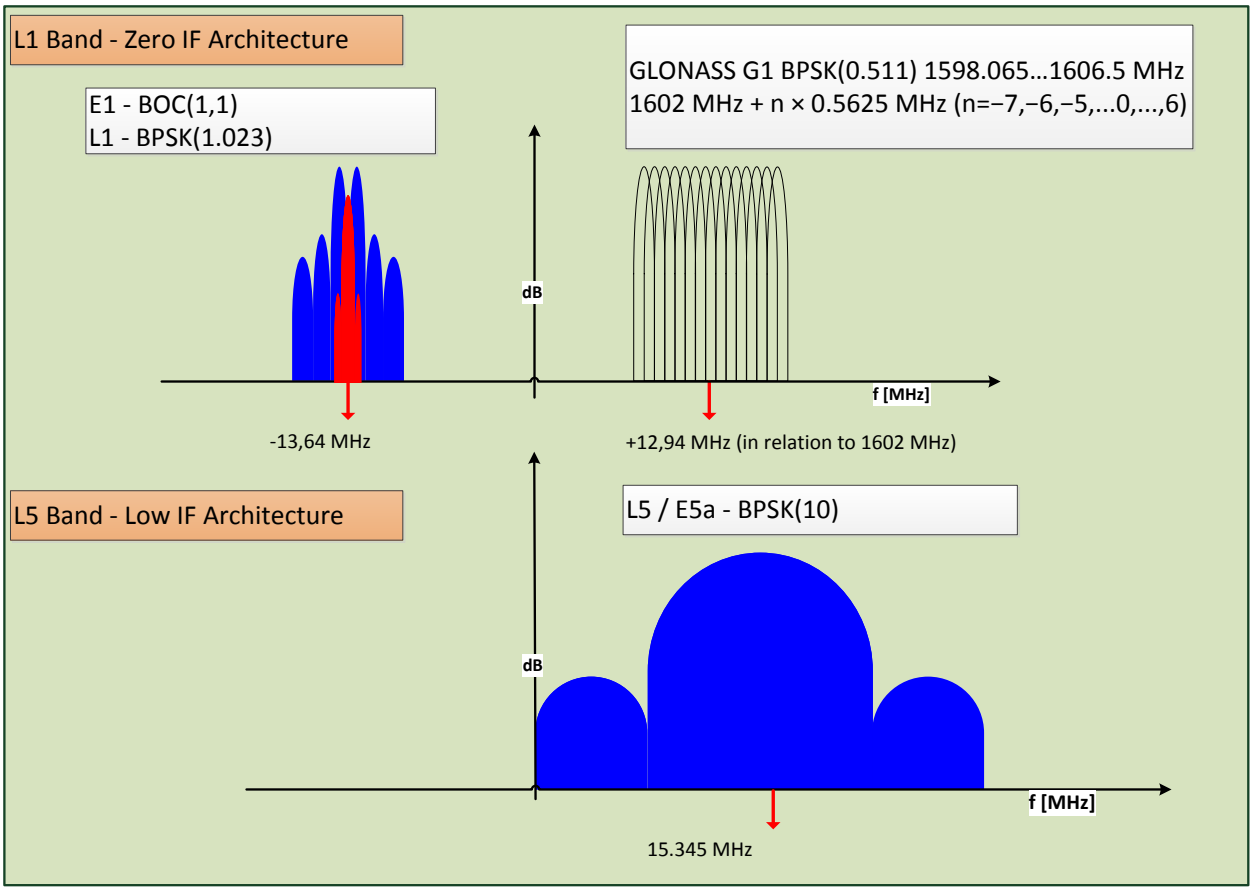

Figure 2. RF front-end frequency plan

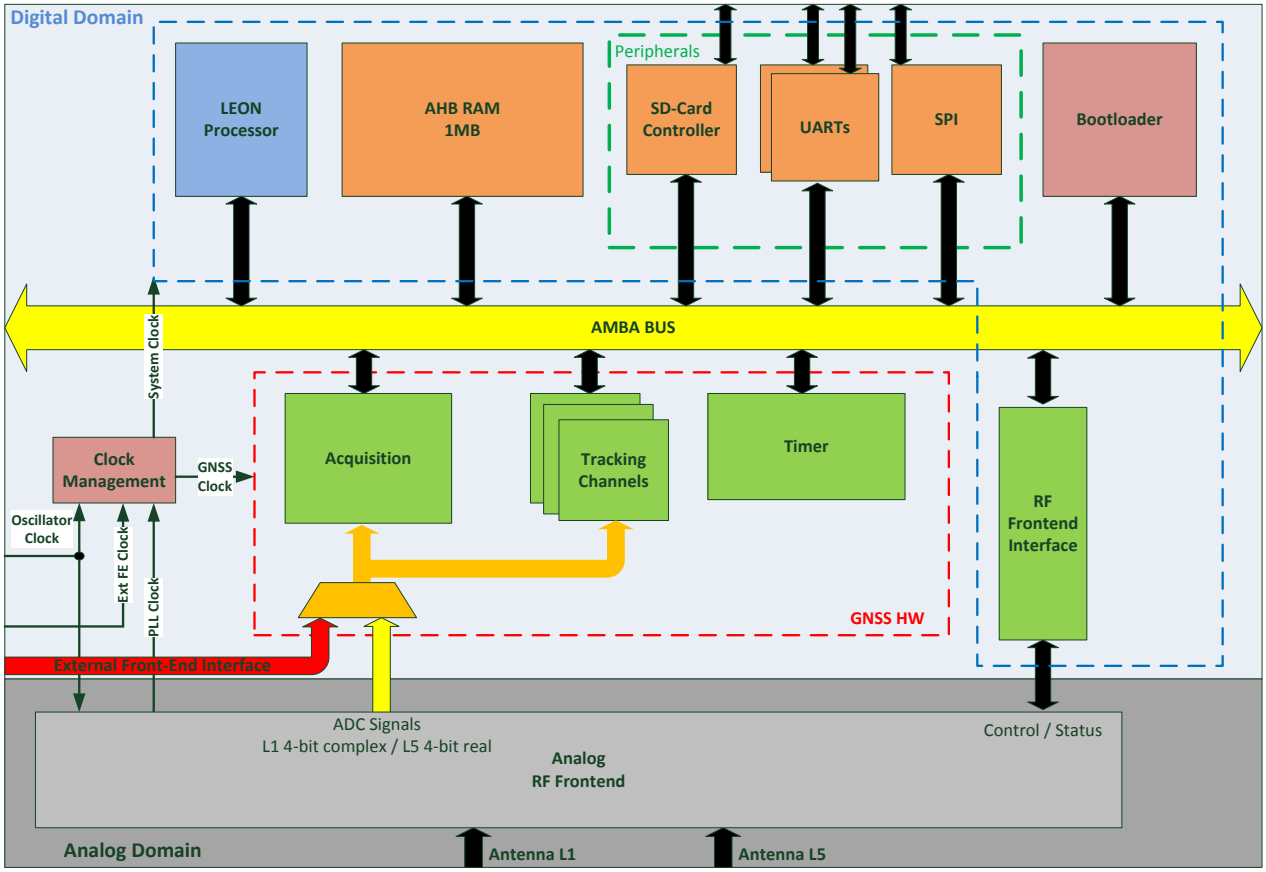

Figure 3. Overall NAPA architecture with emphasis on the digital core blocks

real-time constraints as well as the control and status interface of the RF-front-end. Since the GNSS modules operates in a separate clock domain that runs at half the frequency of the processor domain, some synchronization logic is necessary to ensure correct CDC.

The adoption of a SoC architecture provides a higher flexibility than in conventional static hardware solutions. In addition to typical GNSS applications the user can implement for example some signal monitoring and processing algorithms in software. The eCos [6] embedded operating system is provided in order to ease software development.

1) Generic Peripherals: The digital core is equipped with several peripherals that enable the communication with the outside world. There are two separate universal asynchronous receiver/transmitter (UART) interfaces that can run at 115.2 kbps. A dedicated serial peripheral interface (SPI) master is also provided with maximal 10 MHz clock frequency. These interfaces can be used to provide for example NMEA data to some external display device or raw data (pseudo-ranges, code phases) in order to calculate a PVT solution. It is also possible to access directly the measurements generated from the correlator hardware and to control the tracking NCOs. This way the user can choose his own algorithms for the loop closure. A possible application is the realization of vector delay tracking using the NAPA ASIC and an external processor.

The SD-card interface allows to load and store large amount of data block-wise. Memory codes and Almanacs could be loaded into a SD-card. It is also foreseen the possibility to make signal snapshots periodically and save them to a SD-card for later analysis. This could be useful in special applications where the receiver hardware is not all the time accessible to the user.

In addition, ten general-purpose I/O pins (GPIO) are provided. They can be controlled via software and can provide a very basic interface (for example to connect to external LEDs or switches).

2) Acquisition Module: The acquisition module adopts a parallel code phase search in the Fourier domain by using a 16 kSamples Fast Fourier Transform (FFT) core. The adopted algorithm is known as parallel time-domain search (PTDS) and is described in [7].

The L1/E1/G1 signals coming from the front-end are first filtered and then sent to the acquisition module to allow a fast detection of the satellites in the L1/E1/G1 bands with their respective code delays and Doppler frequencies. The

acquisition of GLONASS G1 FDMA signals is possible thanks to a software-configurable hardware mixer that can be set with the different G1 carrier frequencies. No direct hardware acquisition is supported for the L5 band signals. The tracking of L5 band signals is possible by making an hand-over from L1 band or a Tong-search using the tracking channels.

The acquisition is performed as an iterative process over all the possible satellites and over a set of Doppler values. These values are obtained by dividing the complete range of the possible Doppler variation into bins. The smaller are these bins, the more accurate is the acquisition result, but the more time is required to complete the entire process.

The acquisition has an additional layer of configurability due to the adoption of coherent and incoherent accumulations. These accumulations are supported in hardware but are completely software-controlled. This gives another possibility to get a higher accuracy at the cost of a larger execution time by increasing the amount of accumulations.

In order to speed-up the acquisition we introduced a dedicated logic based on a novel patented algorithm [8]. With this algorithm we are able to detect the Doppler of the L1/E1 satellites present in the signal with an accuracy of 2 Hz. By performing this Doppler search step before the actual acquisition, we are able to generate a list with Doppler values that can be used instead of the bins. This gives more accurate results thanks to inherent accuracy of the algorithm (see Figure 4) and allows to reduce the acquisition time since the amount of Doppler values are usually smaller than the bins. Another advantage of this algorithm is the possibility to detect the change to an indoor context (lack of satellite signals) just looking at the Doppler list and without performing any acquisition.

An additional possibility to speed up the acquisition phase is to search among a reduced set of satellites. This could be achieved by using almanac data stored in the SD-Card.

A single iteration step for the acquisition of a GPS L1 signal requires no more than 1 ms for each accumulated epoch. For a good compromise between accuracy and speed we use typically four epochs of incoherent accumulation, that means approx 4 ms execution time. For Galileo L1 with four incoherent accumulations an iteration step takes approx 16 ms. This time has to be multiplied by the number of satellites and bins to have an estimation of the execution time of the complete process.

3) Integrated Acquisition Memories: The acquisition module is characterized by dedicated memory blocks used for the fast FFT processing. It also provides the possibility to use this on-chip memories to store a snapshot of the incoming signals. In particular, we can store up to 81,920 samples of raw data for the complex L1 and real L5 IF signals for further analysis or processing, even off-chip. This corresponds approximately to 1.1 ms at the frequency of 74.487 MHz. This enables for example sophisticated spoofing detection methods as well as interferer detection and characterization methods. Spoofing detection can be implemented by monitoring the 2D-acquisition search space. Interferer detection and characterization can employ short-time Fourier transforms (STFT) on the snapshot.

It is also foreseen the possibility to use the chip as a simple snapshot receiver without using the on-chip dedicated GNSS hardware anymore. For this purpose the integrated peripherals like UART and SPI ports are provided as interfaces.

4) Tracking Module: The forty versatile tracking channels can be mapped to any combination of GPS, Galileo and GLONASS signals on the two reception bands. One possible combination is e.g. to track simultaneously 10 GPS and 10 Galileo satellites on both L1/E1 and L5/E5a bands. Or, as an alternative, the user can include GLONASS signals by using less GPS / Galileo combinations. The assignment of these tracking channels to the actual GNSS signals can be changed at run-time in order to adapt to different reception situations or to assist the selected signal processing methods.

Each channel is characterized by a 5-tap correlator. For the BPSK modulated signals without side peaks like GPS L1/L5, Galileo E5a and GLONASS G1, we use only three values (Early, Late and Prompt), for Galileo E1 BOC(1,1) signals five values are foreseen (very early and very late in addition to the previous), to be able to detect false peak lock conditions and apply a bump-jumping algorithm. The switch between these modes can be done at run-time and determines the amount of correlation values that are exchanged between correlators and processor.

5) Low-Power Features: The GNSS modules operate in their own clock domain. This clock domain is divided in clock-gated regions. There is a common region for the bus interfaces, one region for the acquisition and one for each tracking channel. This allows a fine-grain shut-down of the GNSS modules that are not currently in use. For example, the acquisition can be deactivated when there are enough signals in tracking or the unused tracking channels can be disabled. This allows a reduced power consumption for the idle modules. This activation/deactivation procedure is controlled through a set of registers connected to the APB and is performed via software.

6) External Front-end Interface: In order to allow a bigger flexibility we provided an additional RF front-end interface. The interface is also depicted in Figure 3. This interface features one 2-bit complex and an additional 2-bit real input, as well as a clock input. The user can decide to directly connect the digital baseband core to an external RF front-end with compatible sampling rate parameters, e.g. [4], and exclude the on-chip RF front-end. This way the NAPA chip can be used for example for the validation of other RF front-end devices or can be adapted to special customer needs.

7) Boot-Up Sequence: The SoC includes a hard-coded bootloader that is in charge of the bus control at start-up. In this phase, the processor is switched off. The bootloader loads a 24 kbyte program from the SD-card to the system memory and starts the processor. In this phase, the processor runs with the external oscillator clock. Having performed the RF front-end initialization the processor can switch to the front-end PLL generated processor clock that runs at approximately

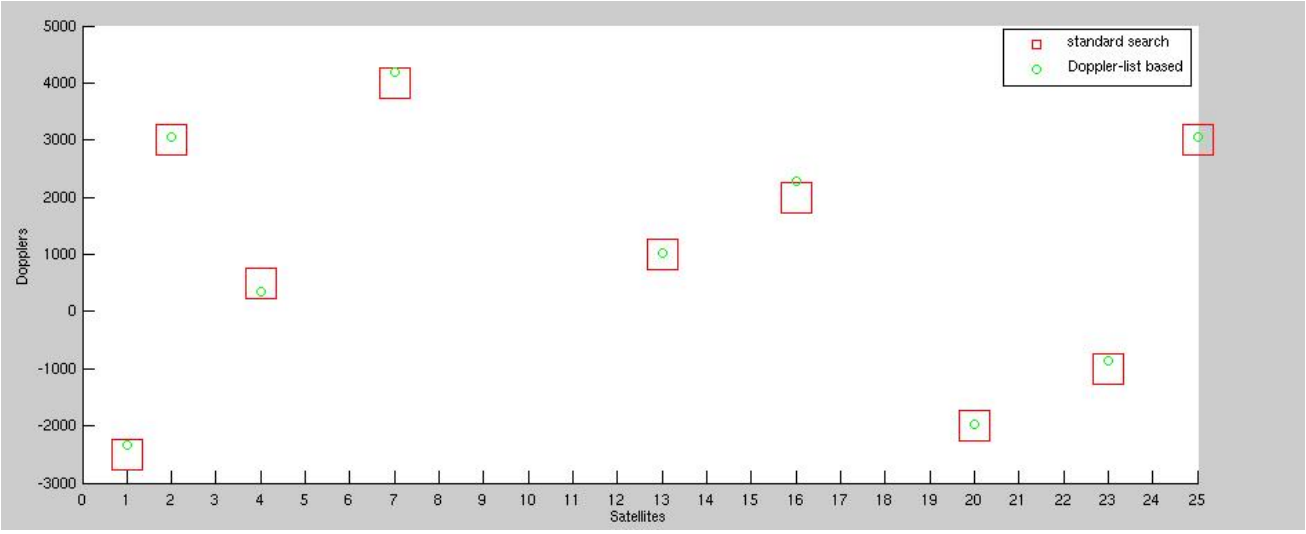

Figure 4. Comparison between standard and Doppler-list based acquisition of a L1 signal

150 MHZ. This switch is completely transparent to the processor. Then the actual main GNSS receiver program is loaded into the system memory and executed.

III. The NAPA chip

The NAPA chip has been manufactured in a low-power 1.2 V 65 nm TSMC technology. The 4.5 mm x 5.0 mm chip die was mounted in a QFN68 package and first test samples are available. The core requires a 1.2 V power supply, the pads 1.8 V. The static power consumption is equal to approx 0.4 mW. The processing of the *Paranoia* floating-point test suite using the SPARC Leon processor at 150[MHz] requires 50 mW. The simultaneous tracking of 10 satellites requires 127 mW.

Figure 5 shows a picture of the die and its interconnections. The two parts, the analog core and the digital baseband, are clearly distinguishable. The chip is currently in the verification phase.

Within the project the development and testing of the NAPA design was carried out on basically two platforms. During the hardware development phase, the baseband core has been prototyped on a FPGA device and tested using a special file player setup explained in the following section. Having taped-out the chip and received the first samples from the foundry a test board has been developed in order to verify the NAPA chip functionality.

A. FPGA Test Setup

In the development phase the NAPA baseband core has been implemented on a Xilinx Virtex6 FPGA device. A Xilinx ML605 development board [9] has been used for the test setup. The main limitation of the testing in this phase was the lack of a prototype of the analog RF front-end. In order to allow the early testing of GNSS functionality we adopted a *file player* developed by Fraunhofer IIS in a previous project [10]. This *file player* uses a desktop PC to reproduce a digital

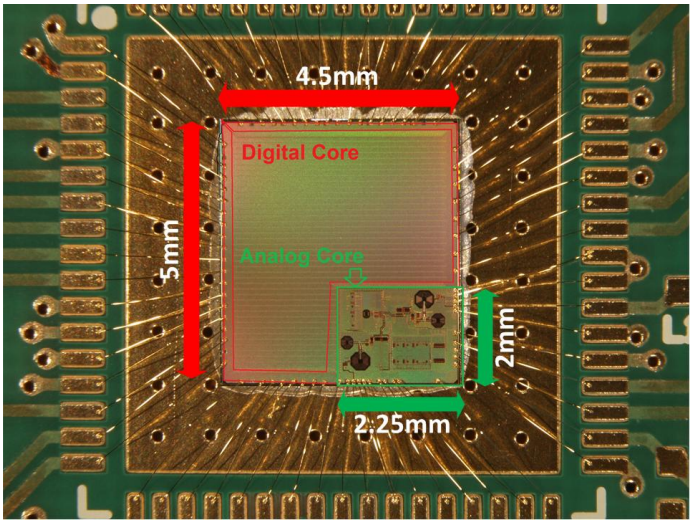

Figure 5. NAPA Chip

signal data-stream stored in a binary file on the PC. This stream is sent through a dedicated interface to a commercial digital acquisition board [11]. This board receives a clock synchronized with the clock of the baseband core in the FPGA and delivers the signals directly to the FPGA pins. The complete setup is depicted in Figure 6. The setup in use can be seen on the left part of Figure 7.

B. Test board

In the verification phase still ongoing, the first unpackaged test chip dies have directly been glued to the test PCB and bonded on board without any housing. After receiving the packaged chips the QFN68 could be regularly soldered on the PCB. A block diagram of the board is depicted in Figure 8. The board hosts the typical switch buttons and LEDs for quick control and status detection as well as some specific interfaces. The clock can be provided through a dedicated SMA clock

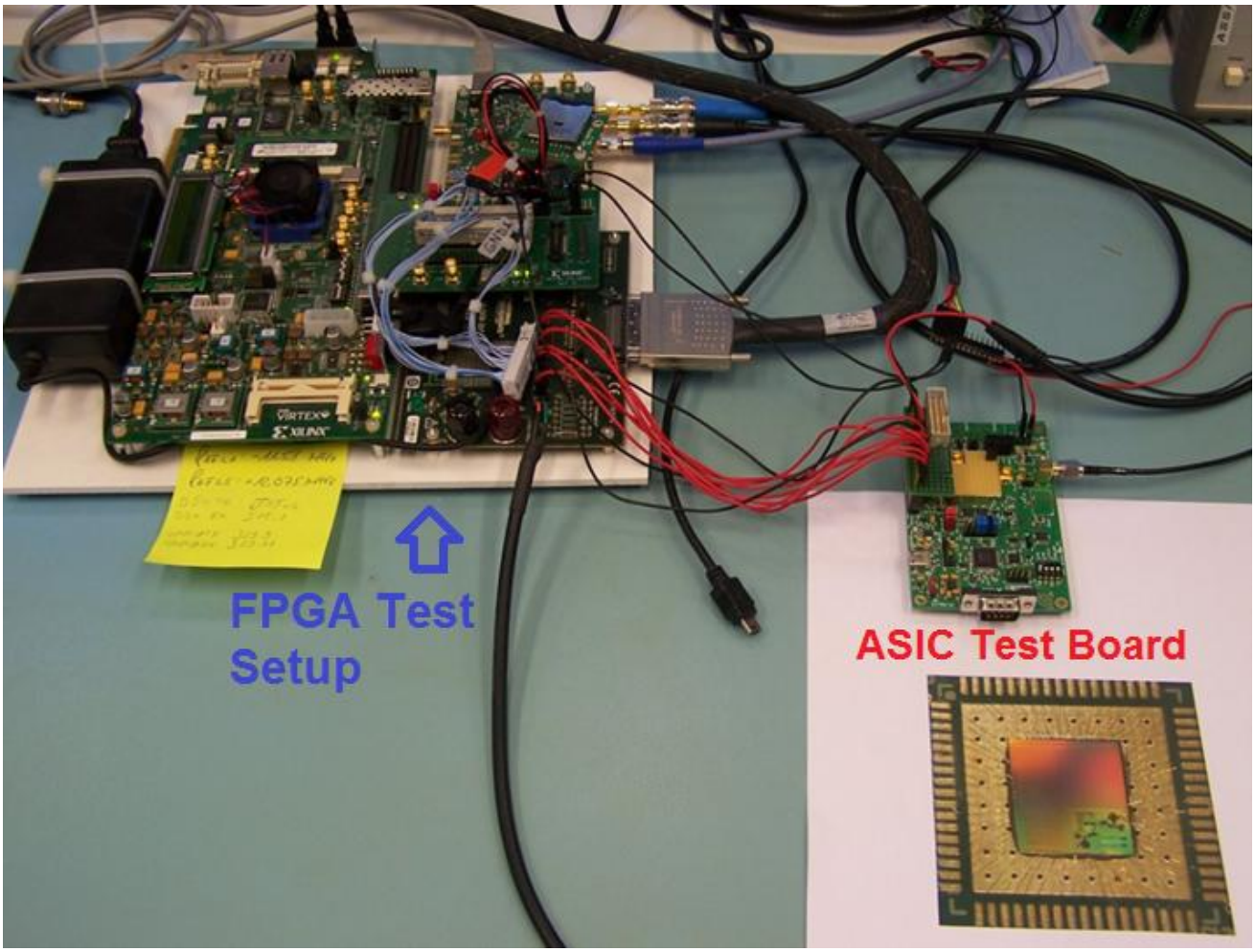

Figure 7. FPGA test setup and ASIC test-board in use

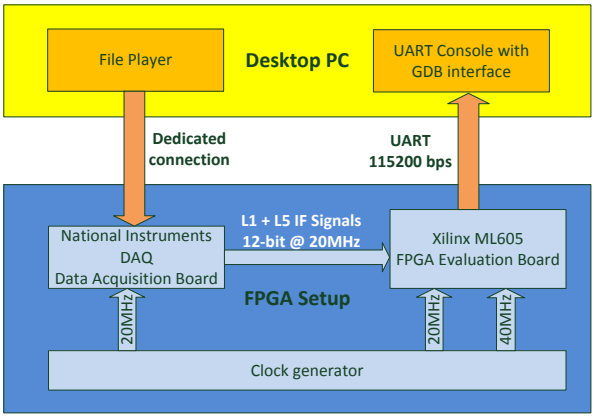

Figure 6. FPGA Test Setup

connector as well as a discrete oscillator. Two Sub-Miniature-Push-on (SMP) connectors are also provided for separate the L1 and L5 antenna inputs. The two UART ports, the debugger UART and the SPI master port are connected using a FTDI chip [12]. This chip allows the simultaneous connection of these ports to a desktop PC USB port. A parallel connector is provided to interface external front-end ADC signals and clock. Through the same connector the GPIOs are accessible. A dedicated socket is added for a mini SD-card.

C. Preliminary Results

The chip on the test board has been tested first using the same *file player* of the FPGA setup (Figure 7 on the bottom-right corner). This way we could evaluate the correct functionality of the digital baseband core without the need to activate and configure the on-chip front-end. After the successful tests, we focused on the on-chip front-end configuration and we used the antenna connectors to provide valid GNSS signals. We tested the chip using three different configurations: a GNSS signal simulator, a static roof antenna and a small active patch antenna.

In the three configurations, we could successful acquire and track GPS L1 and Galileo E1 signals. The tracking of L5 and E5a signals was not possible with the on-chip frontend but was achieved using an external frontend. This revealed a bug

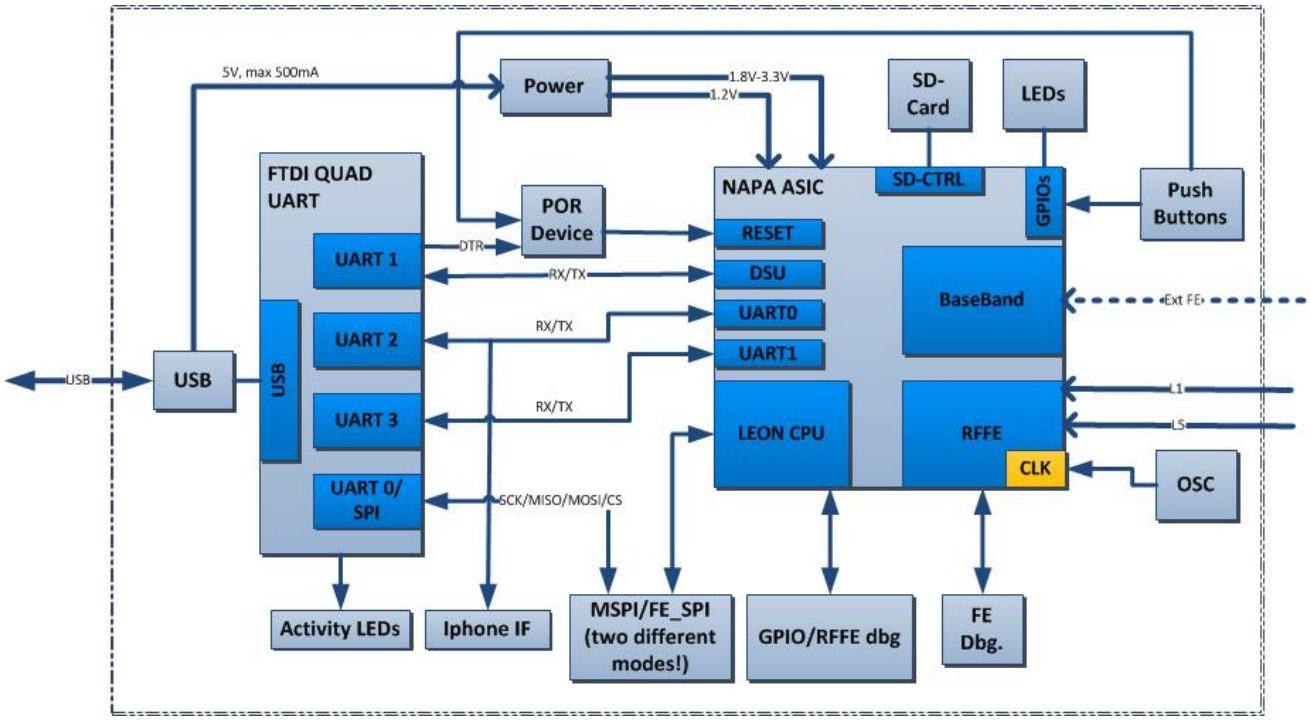

Figure 8. Block diagram of NAPA test board

in the on-chip frontend that made necessary a redesign of the analog core.

Figure 9 shows the spectrum of a snapshot of L1 and L5 paths made using the on-chip dedicated snapshot hardware and sent through the UART port with a dedicated binary protocol for offline processing. For this special test we used an arbitrary waveform generator to provide Galileo and GLONASS signals without noise in the L1 and L5 frequency bands supported by the NAPA chip. After performing a FFT of the two snapshots, we can clearly see these signals. In the L1 plot, the E1b signal is present in the negative frequency range with the two peaks typical of the BOCsin(1,1) modulation. The FDMA GLONASS G1 is in the positive frequency range with his trapezoidal characteristic. It is also possible to see a peak of the E1a BOCcos(15,2.5) in the proximity of the zero frequency. In the L5 plot we can see the main peak of BPSK E5a signal on the right and its mirrored image on the left, due to the fact that L5 signal path is real.

IV. Conclusion

In this paper we presented NAPA, a fully integrated, multi-constellation dual-frequency single-chip GNSS receiver. This chip includes an analog RF front-end and a digital baseband core with an embedded 32 bit microcontroller. The front-end supports the simultaneous reception of GPS L5 / Galileo E5a and GPS L1 / Galileo E1 / GLONASS G1 signals as well as modes where only one reception path is activated. The baseband core allows acquisition and tracking of the supported signals using a hardware/software integrated approach. An acquisition module and forty 5-tap hardware correlators are controlled by an integrated SPARC compatible, LEON2 embedded processor that takes care also of the tracking loops closure. A 1 MBytes on-chip memory is provided to host the main program. An SD-card interface allows the load and store of larger amount of data. Several I/O interfaces are provided to allow the communication with the outside world. The chip can be used as a standard multi-constellation dual-frequency receiver but the provided flexibility allows also its employment as GNSS sensor or snapshot receiver. The chip has been manufactured in a low-power 1.2 V 65 nm TSMC technology. The baseband core has been prototyped during development on a Virtex6 FPGA device. A special test-setup has been used to evaluate the baseband functionality without using any external front-end. A dedicated test-board has been designed for the test chips. The chip has been verified using a GNSS signal simulator, a static roof antenna and a small active patch antenna. In the three configurations, we could successful acquire and track GPS L1 and Galileo E1 signals. The tracking of L5 and E5a signals was not possible with the on-chip frontend but was achieved using an external frontend. This revealed a bug in the on-chip frontend that made necessary a redesign of the analog core.

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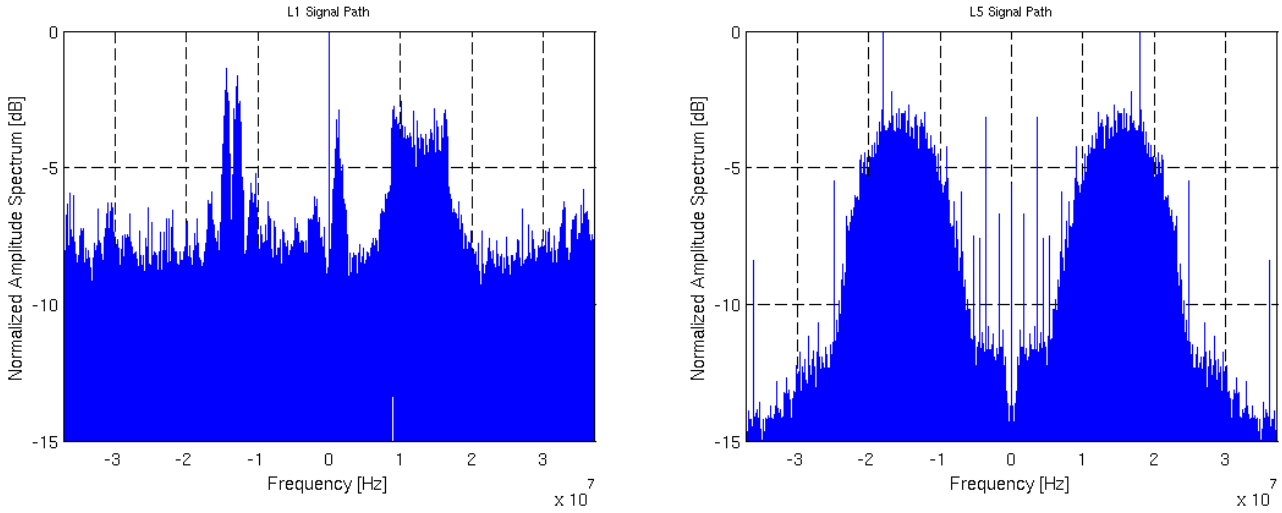

Figure 9. Spectrum of a L1 and L5 signal snapshot

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