Fraunhofer IIS

ADELIA Gen2 Analog Deep Learning Inference Accelerator

Energy-saving AI ASIC for the 22FDX® and TSMC 90nm technology

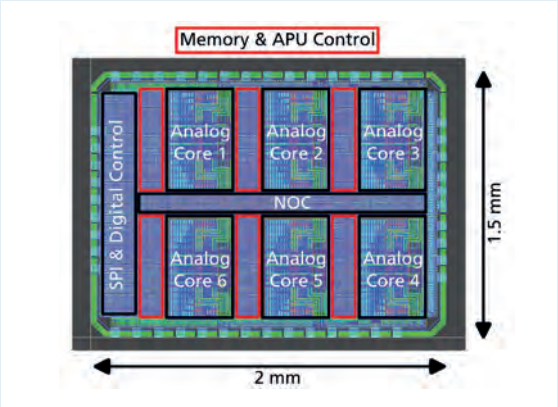
ADELIA is a new analog AI accelerator technology developed by Fraunhofer IIS to significantly enhance the energy efficiency and latency of AI systems. The innovative architecture relies on analog rather than digital computation methods, enabling faster AI model execution with lower energy consumption. This is particularly beneficial for mobile and embedded systems where resources are limited. The technology can be integrated with standard semiconductor processes, ensuring broad industrial applicability while minimizing costs.

Key Facts

- Configurable and scalable multi-core architecture
- Mixed-signal design with analog crossbar
- Highly parallel execution of MAC operation for convolutional and fully connected layers
- Support of established qualified semiconductor processes (e.g. GlobalFoundries 22FDX®, TSMC 90nm)
- Optimized hardware-software co-design flow for IP core design
- Toolchain for deployment of AI models post-production

Benefits

- **Energy Efficiency:** ADELIA's analog-digital architecture reduces power consumption by up to 90 % compared to traditional digital accelerators. This makes it ideal for battery-powered devices.
- **Ultra-Low Latency:** ADELIA's high-speed processing enables real-time applications that demand rapid responses. This is crucial for tasks like real-time analytics.
- **Software-Toolchain:** ADELIA comes with a powerful software development kit that simplifies the optimization and deployment and optimization of neural networks.
- **Versatility:** ADELIA is highly versatile and can be used for a variety of AI applications, including image and speech recognition, natural language processing, and medical diagnostics. Adaptation to customer requirements is easy to implement.



ADELIA Gen2 Layout in 22FDX®
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KPI improvement for voice activity detection use case:
ADELIA performance compared to a conventional microcontroller

KPI	ADELIA	MCU	Improvement
Latency	1 ms	78 ms	> 78x
Power	0,260 mW	66 mW	> 250x
Energy	0,260 µJ / Inference	5163 µJ / Inference	> 19 000x

Hardware-Software Co-Design Flow

An optimized hardware-software co-design approach captures the use case requirements of ADELIA. This process ensures rapid functional adjustments and porting, streamlining the development process. Furthermore, it allows the deployment of AI models post-production accommodating potential changes in the usage of ADELIA.

Use Case Example: Voice Activity Detection

One concrete implementation of ADELIA in 22FDX® realized a voice activity detection use case. The outcome of this project is highlighted through the following features:

- Small area for low price: 3 mm² with 6 processing units
- Software-grade accuracy (meaning within ± 3 % of the software solution's accuracy)
- Measured efficiency: ~ 5.5 TOPS/W

Further Applications

- **Wearables:** AI wearables with local data protection-compliant data processing, offering high comfort through a compact form factor and long battery life.
- **IoT:** Sensor-near intelligent data classification with unmatched battery life – even within control loops.
- **Healthcare:** Mobile local network-independent AI data processing, offering high comfort through a compact form factor and high reliability.

Our Offer: Energy-efficient Smart Chip Design

With our extensive network of universities, research institutions, and industrial partners, we bridge the gap between the latest technology trends and industry-standard applications.
We identify, develop, and implement the appropriate neuro-morphic design for each use case. Our offering includes:

- Feasibility studies
- Inference accelerator IPs
- Sensor ASICs with NPU
- Access to foundries for small volume production

Additional offers:

- ADELIA Evaluation Kit
- SENNA: ultra-fast Spiking Neural Network processor
- Co-Integration with RISC-V processors

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