Mini@sic Schedule 2020

Version 200212 – v2

EUROPRACTICE
IC SERVICE
www.europractice-ic.com

2020 MINI@SIC EUROPRACTICE MPW RUN SCHEDULE AND PRICELIST

Picture: imec

Mini@sic solution allows to prototype particularly small designs at low prices on selected MPW runs. It is accessible for universities, research institutes and companies.

Mini@sic Solution

- GLOBALFOUNDRIES
  selected MPW runs for 130nm, 55nm, 45nm and 22nm
- IHP
  all MPW runs
- ON Semiconductor
  all MPW runs for 0.7µm and 0.35µm
- TSMC
  selected MPW runs for 0.18µm, 65nm, 40nm and 28nm
- UMC
  selected MPW runs for 0.18µm, 0.13µm and 65nm
- X-FAB
  selected MPW runs for XH018 and XT018

Microblock Solution

- TSMC
  selected MPW runs for 28nm HPC and HPC+

MINI@SIC

Through the mini@sic program, the EUROPRACTICE-IC Service offers special MPW prototyping conditions in order to stimulate academia and publicly funded research institutes to prototype small ASIC designs for educational or research purposes.

Although our General Multi-Project-Wafer services allow to share the high cost of a prototype run (masks and wafers) among several customers, the minimum prototyping charges remain too high for most academic clients. Therefore, EUROPRACTICE offers considerably lower minimum prototyping charges by introducing the mini@sic concept for small ASIC designs. Several times per year, a minimum area MPW block size is bought and resold in smaller sub-blocks. This solution offers lower prototype fabrication costs than standard MPW runs.

Academia and Research Institutes together with small and medium-sized enterprises have now the possibility to prototype particularly small designs at low prices on selected MPW runs.

MICROBLOCK

EUROPRACTICE-IC offers its customers a particularly small silicon area of one mm^2 to fabricate their designs in the TSMC 28nm HPC and HPC+ technology. This so-called Microblock can be placed on any of the 28nm Multi-Project-Wafer (MPW) runs that use the mini@sic methodology.

- Designed area: 1110µm x 1110µm.
- Lead time of 106 days, including tapeout preparation.
- 100 parts per participation.
- Full PDK and library support.
- 2 runs per year with timing tuned towards key conferences.

GLOBALFOUNDRIES

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
GLOBALFOUNDRIES 130nm BCDlite			9						1			
GLOBALFOUNDRIES 55 nm Lpe				20						5		
GLOBALFOUNDRIES 45RFSOI										5		
GLOBALFOUNDRIES 22 nm FDSOI			9				13				2	

Important notes: Dates are **Registration** deadlines after which designs cannot be accepted. Final GDSII file must be submitted within **6 weeks** after this date.
A **cancellation fee** is applicable if the registration is cancelled later than 2 weeks after the Registration deadline or if the customer is unable to provide a DRC-clean GDS before the Tapeout deadline.
We reserve the right to cancel mini@sic runs if the run is not economically feasible.
mini@sic participation is possible only with mandatory metal stack and inline wirebond.
Dates in red are preliminary.

IHP

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
IHP SGB25V 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 75/95GHz, 5M/MIM, breakdown voltages up to 7V		7					24					
IHP SG25H3 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 110/180GHz, 5M/MIM, breakdown voltages up to 7V		7					24					
SG25H5_EPIC Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + Photonics				17						23		
IHP SG25 PIC (Photonics, Ge Photo-diode, BEOL)							17					
IHP SG13S SiGe:C Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + optional TSV	10		20			19			4			
IHP SG13C SiGe:C CMOS 7M/MIM	10		20			19			4			
IHP SG13G2 SiGe:C Bipolar/Analog, Ft/Fmax= 300/500GHz, 7M/MIM + optional TSV	10		20			19			4			
IHP SG13G2Cu FEOL process SG13G2 together with Cu BEOL option			20			19*			4			
IHP SG13SCu FEOL process SG13S together with Cu BEOL option			20			19*			4			
IHP BEOL SG13 (M1 and Metal Layers Above) + optional LBE or TSV			6									

Important notes: Dates are **Registration** deadlines. DRC clean GDSII file must be submitted within **10 days** after this date.
* Additional MPW runs offered only when the cumulative area > 10mm².
Bumping is available for all IHP technologies with extra charge, limited to 200 bumps.

ON Semiconductor

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
ON Semi 0.7µ C07M-D 2M/1P & ON Semi 0.7µ C07M-A 2M/1P/PdiffC/HR	3		23			2		10		26		
ON Semi 0.7µ C07M-I2T100 100V - 2M & 3M options	3		23			2		10		26		
ON Semi 0.35µ C035U - 4M (3M & 5M optional) only thick top metal	27			14			1		14			1
ON Semi 0.35µ C035 - I3T25U 3.3/25V 4M (3M & 5M optional) only thick top metal	27			14			1		14			1
ON Semi 0.35µ C035 - I3T80U 80V 4M - 3M optional (5M on special request)	2			1			6			5		
ON Semi 0.35µ C035 - I3T50U (E) 50V 4M - 3M optional (5M on special request)			2		25				1			1

Important notes: Dates are **GDS submission** deadlines. Design registration must be done at least **3 weeks** in advance.

TSMC

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
TSMC 0.18 CMOS Logic or Mixed-Signal/RF, General Purpose	22				13				23			
TSMC 0.18 CMOS High Voltage BCD Gen II				8						28		
TSMC 65nm CMOS Logic or Mixed-Signal/RF, Low Power*		19			13			19			18	
TSMC 40nm CMOS Mixed-Signal/RF, Low Power				15					30			
TSMC 28nm CMOS RF HPC*			18							28		
TSMC 28nm CMOS RF HPC - Microblock*			18							28		
TSMC 28nm CMOS RF HPC+*							1					
TSMC 28nm CMOS RF HPC+ - Microblock*							1					

Important notes: Dates are **GDS submission** deadlines. Design registration must be done at least **4 weeks** in advance unless otherwise specified in the table above.
*For these technologies, please make reservation **4 months** in advance.
Bumping is available upon request for all 12-inch technologies.
Contact eptsmc@imec.be if any of the following options are used:
Bumping, MTP/OTP, Deep Trench, High Linearity MiM, Schottky Barrier Diode, ULL N/PMOS.
Dates in red are preliminary.

TSMC mini@sic Options

Options mini@sic Runs	IO	MIM/um2	Remarks
TSMC 0.18 CMOS Logic or Mixed-Signal/RF, General Purpose	3.3 V	2 fF	Metal scheme: 1P6M_4X1U with UTM (20kA) topmetal
TSMC 0.18 CMOS High Voltage BCD Gen II	5V	2 fF between M5 & M6	Voltage: 1.8/5/6/8/12/16/20/24/29/36/45/55/65/70V/Vg1.8/5V Metal scheme: 1P6M_4X1U with UTM (30kA) topmetal No deep trench support
TSMC 65nm CMOS Logic or Mixed-Signal/RF, Low Power	2.5V (1.8UD, 3.3OD)	2 fF	Core : 1.2 V, Metal scheme : 1P9M_6X1Z1U_RDL Default : wirebond with 14kA thick RDL.AP layer mandatory in bondpads.
TSMC 40nm CMOS Mixed-Signal/RF, Low Power	2.5V (1.8UD, 3.3OD)		Core : 1.1 V (no triple gate oxide!) Metal scheme : 1P8M_5X2Z_RDL. Default : wirebond with 14kA thick RDL.AP layer mandatory inbondpads.
TSMC 28nm CMOS RF HPC (+) – also applies for Microblock	1.8 V		Core : 0.9 V, Metal scheme : 1P8M_5X1Z1U UTRDL (28kA thick AP layer) Default: BEOL option 1, 11 mils backlapping

UMC

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
UMC L180 Mixed-Mode/RF	27			20			20		21			7
UMC L130 Mixed-Mode/RF		17				22				26		
UMC L65N Logic/Mixed-Mode/RF - LL		17					27					7

Important notes: Dates are **GDS submission** deadlines. Design registration must be done at least **3 weeks** in advance.
Dates in red are preliminary.

UMC mini@sic Options

Options mini@sic Runs	Metalization	Core	IO	MIM	Topmetal	Remarks
UMC L180 Mixed-Mode/RF	1P6M	1.8V	3.3V	1fF	20kA	
UMC L130 Mixed-Mode/RF	1P8M2T	1.2V	3.3V	1fF	20kA	Possible combinations: HS, HS-LL (No SP possible)
UMC L65N Logic/Mixed-Mode/RF - LL	1P8M1T0F1U	1.2V	2.5V/2.5V_OD3.3V	2fF	32.5kA	Metal-stack "26".

Technology	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
XH018 0.18µ HV NVM CMOS E-FLASH				17						23		
XT018 0.18µ HV SOI CMOS			16								2	

Important notes: Dates are **GDS submission** deadlines. Design registration must be done at least **2 weeks** in advance.

X-FAB mini@sic Options

Options mini@sic Runs	Process modules included for 4 metal options
XH018 0.18µ HV NVM CMOS E-FLASH	LPMOS, MET3, MET4, METMID, METTHK, MRPOLY, ISOMOS, LVT, DMOS, HVMOS, SCHOTTKY, MIM, NVM, FLASH, OTP3, PHOTODIO
XT018 0.18µ HV SOI CMOS	LP5MOS, HVN, HVP, 1XN, 1XP, PSUB, DTI, DNC, DPC, NBUR, HRPOLY, MIMH, MET3, MET4, METMID, METTHK, HWC

EUROPRACTICE
IC SERVICE
www.europractice-ic.com

2020 PRICELIST FOR MINI@SIC EUROPRACTICE MPW RUNS

Prices are valid for General EUROPRACTICE MPW runs from 1 January 2020
Prices and conditions are subject to modification at any time without prior notice.

Discounted price

Three conditions for discounted prices:

- A customer represents an academic institution or a research facility from one of the 28 EU countries together with Albania, Armenia, Azerbaijan, Belarus, Bosnia-Herzegovina, Georgia, Iceland, Israel, Liechtenstein, North Macedonia, Moldova, Montenegro, Norway, Russia, Switzerland, Turkey, Serbia and Ukraine.
- A customer is a registered EUROPRACTICE member who has paid the Full-IC annual membership fee.
- The intended design will be done for educational purposes or for publicly funded research.

Standard price

Standard prices apply to all other customers.

Number of prototypes

GLOBALFOUNDRIES: 25 samples
IHP: 40 samples SG25 & SG13,
25 samples using TSV module, PIC & EPIC
ON Semi: > 20 samples
TSMC: 40 samples for 0.18µm,
100 samples for 65nm and 28nm
UMC: 25 samples for 0.18µm and 0.13µm
50 samples for 65nm
X-FAB: 50 samples

If you need more prototype samples, please contact us for a quotation.

Plots

You can order plots/PDF of your designs:

- First plot/PDF costs 50 euro
- Next plots cost 20 euro each

Packaging

Prices are given for the delivery of unpackaged, untested prototypes. Encapsulation and testing will be charged separately.

See separate prices and available packages on europractice-ic.com/schedules-prices/

GLOBALFOUNDRIES

Technology	Standard EUR / block	Discounted EUR / block
GLOBALFOUNDRIES 130 nm BCDlite	5,900 [1]	4,900 [1]
GLOBALFOUNDRIES 55 nm LPe	11,900 [2]	9,900 [2]
GLOBALFOUNDRIES 45RFSOI	20,900 [2]	17,900 [2]
GLOBALFOUNDRIES 22 nm FDSOI	29,900 [3]	24,900 [3]

Important notes: [1] Price = per block of 1750µm x1750µm needed to fit the design in. The mentioned die size is referred to the Pre-Shrink die size.

[2] Price = per block of 1500µm x 1500µm needed to fit the design in. The mentioned die size is referred to the Pre-Shrink die size.

[3] Price = per block of 1250µm x 1250µm needed to fit the design in. The mentioned die size is referred to the Pre-Shrink die size.

IHP

Technology	Standard EUR / mm²	Discounted EUR / mm²
IHP SGB25V 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 75/95GHz, 5M/MIM, breakdown voltages up to 7V	2,125 [1,2]	2,000 [1,3]
IHP SG25H3 0.25µ SiGe:C Bipolar/Analog, Ft/Fmax= 110/180GHz, 5M/MIM, breakdown voltages up to 7V	3,230 [1,2]	3,040 [1,3]
SG25H5_EPIC Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + Photonics	6,800 [1,2]	4,800 [1,3,5]
IHP SG25 PIC (Photonics, Ge Photo-diode, BEOL)	3,230 [1,2]	2,660 [1,3]
IHP SG13S SiGe:C Bipolar/Analog, Ft/Fmax= 250/300GHz, 7M/MIM + optional TSV	5,355 [1,2]	4,410 [1,3]
IHP SG13C SiGe:C CMOS 7M/MIM	3,825 [1,2]	3,600 [1,3]
IHP SG13G2 SiGe:C Bipolar/Analog, Ft/Fmax= 300/500GHz, 7M/MIM + optional TSV	6,205 [1,2]	5,110 [1,3]
IHP SG13G2Cu FEOL process SG13G2 together with Cu BEOL option	5,950 [1,2]	5,000 [1,3]
IHP SG13SCu FEOL process SG13S together with Cu BEOL option	5,185 [1,2]	4,360 [1,3]
IHP BEOL SG13 (M1 and Metal Layers Above) + optional LBE or TSV	850 [1,2]	800 [1,3]
IHP Special Services		
Bumping (available for all IHP technologies)	6,500 [2,4]	4,700 [3,4]
Localized Back side Etching (available for all IHP technologies) not offered for EPIC/PIC runs	4,250 [2,4]	2,500 [3,4]
TSV to ground (SG13)	4,250 [2,4]	2,500 [3,4]
Non-Standard wafer thickness in SG13	3,000 [2,4]	3,000 [3,4]
Non-Standard wafer thickness in SG25	2,000 [2,4]	2,000 [3,4]

Important notes: [1] Price = area (mm2) * price/mm² with min. fabrication cost equivalent to 0.8mm². The chip area is inclusive of the filler cells outside the seal ring.
[2] Price for designs created for educational purposes or publicly funded research for **non-EU countries**.
[3] Price for designs created for educational purposes or publicly funded research for the **EU countries**.
[4] One-off fee.
[5] Special introductory price.

ON Semiconductor

Technology	Standard EUR / mm²	Discounted EUR / mm²
ON Semi 0.7µ C07M-D 2M/1P	300	270
ON Semi 0.7µ C07M-A 2M/1P/PdiffC/HR	350	315
ON Semi 0.7µ C07M-I2T100 100V - 2M	525	485
ON Semi 0.7µ C07M-I2T100 100V - 3M	560	525
ON Semi 0.35µ C035U 4M (default) including analog options	720	670
ON Semi 0.35µ C035U 3M (optional) including analog options	700	650
ON Semi 0.35µ C035U 5M (optional) including analog options	800	750
ON Semi 0.35µ C035 - I3T80U 80V 3M	850	800
ON Semi 0.35µ C035 - I3T80U 80V 4M	925	875
ON Semi 0.35µ C035 - I3T80U 80V 5M	1,050	995
ON Semi 0.35µ C035 - I3T50U (or E) 50V 3M	850	800
ON Semi 0.35µ C035 - I3T50U (or E) 50V 4M	925	875
ON Semi 0.35µ C035 - I3T50U (or E) 50V 5M	1,050	995
ON Semi 0.35µ C035 – I3T25U 3.3/25V 3M (optional)	750	700
ON Semi 0.35µ C035 – I3T25U 3.3/25V 4M (default)	770	720
ON Semi 0.35µ C035 – I3T25U 3.3/25V 5M (optional)	800	750

Important notes: Price = area (mm²) * price/mm² with min. fabrication cost equivalent to 4 mm².

Technology	Standard EUR / block	Discounted EUR / block
TSMC 0.18 CMOS Logic or Mixed-Signal/RF, General Purpose [7]	3,100 [1]	2,640 [1]
TSMC 0.18 CMOS High Voltage BCD Gen II [8]	5,050 [2]	4,430 [2]
TSMC 65nm CMOS Logic or Mixed-Signal/RF, Low Power [9]	12,550 [3]	11,820 [3]
TSMC 40nm CMOS Mixed-Signal/RF, Low Power [10]	16,880 [4]	15,880 [4]
TSMC 28nm CMOS RF HPC [11]	15,850 [5]	13,650 [5]
TSMC 28nm CMOS RF HPC - Microblock [6]	9,750	7,650
TSMC 28nm CMOS RF HPC+ [11]	15,850 [5]	13,650 [5]
TSMC 28nm CMOS RF HPC+ - Microblock [6]	9,750 [6]	7,650 [6]

Important notes: [1] Price = per block of 1660µm x 1660µm needed to fit the design in.
[2] Price = per block of 2500µm x 2500µm needed to fit the design in.
[3] Price = per block of 2000µm x 2000µm needed to fit the design in.
[4] Price = per block of 1920µm x 1920µm (designed area – pre-shrink) needed to fit the design in; on silicon area – after shrink = 1730µm x 1730µm (see below).
[5] Price = per block of 1570µm x 1570µm (designed area – pre-shrink) needed to fit the design in; on silicon area – after shrink = 1413µm x 1413µm (see below).

[6] Microblock rules applicable to TSMC 28nm

The Microblock size is 1110µm x 1110µm (designed area – pre-shrink). On silicon area is 1000µm x 1000µm.
If the design is larger than the Microblock size, the only option is a mini@sic block.
Multiple Microblocks are possible on one run.
Combining mini@sic and Microblock on one run is also allowed.
Microblock and mini@sic **reservations/registrations** should be done no later than 4 months before the deadline.
Withdrawal of the Microblock or mini@sic block later than one week before the deadline is subject to a penalty of 50% of the amount due. (However, the amount can be recovered at the next participation. In case of two subsequent late withdrawals, the fee cannot be recovered anymore.)
For Microblock, there is no commitment that the run will be launched in case of insufficient number of participations.
For mini@sic, the run will be launched in any case, regardless of the number of participants.

[7] TSMC 0.18µ CMOS mini@sic rules

When the standard block of 5mm x 5mm is divided into 9 regular square sub-blocks, customers participating in the mini@sic program can submit one sub-block or multiple sub-blocks, depending on the size of their design:

- single sub-block: design may not be larger than 1660µm x 1660µm
- 2 sub-blocks: design may not be larger than 3320µm x 1660µm
- 3 sub-blocks: design may not be larger than 4980µm x 1660µm
- 4 sub-blocks: design may not be larger than 3320µm x 3320µm
- 6 sub-blocks: design may not be larger than 4980µm x 3320µm

[8] TSMC 0.18µ HV BCD mini@sic rules

For the mini@sic program, customers can submit one sub-block or multiple sub-blocks, depending on the size of their design:

- single sub-block: design may not be larger than 2500µm x 2500µm
- 2 sub-blocks: design may not be larger than 5000µm x 2500µm

Final price = number of sub-blocks needed to fit in the design * sub-block price.

[9] TSMC 65nm mini@sic rules

For the mini@sic program, customers can submit one sub-block or multiple sub-blocks, depending on the size of their design:

- single sub-block: design may not be larger than 2000µm x 2000µm
- sub-blocks: design may not be larger than 4000µm x 2000µm

[10] TSMC 40nm mini@sic rules

For the mini@sic program, customers can submit one sub-block or multiple sub-blocks, depending on the size of their design:

- single sub-block: design may not be larger than 1920µm x 1920µm (pre-shrink)
- 2 sub-blocks: design may not be larger than 3840µm x 1920µm

These are designed dimensions. Fabricated designs (40nm) are shrunk during mask making in both X and Y directions by 0.9.

[11] TSMC 28nm mini@sic rules

For the mini@sic program, customers can submit one sub-block or multiple sub-blocks, depending on the size of their design:

- single sub-block: design may not be larger than 1570µm x 1570µm (pre-shrink)
- 2 sub-blocks: design may not be larger than 3140µm x 1570µm

These are designed dimensions. Fabricated designs (28nm) are shrunk during mask making in both X and Y directions by 0.9.

UMC

Technology	Standard EUR / block	Discounted EUR / block
UMC L180 Mixed-Mode/RF - 1P6M - 1.8V/3.3V [3]	3,070 [1]	2,570 [1]
UMC L130 Mixed-Mode/RF - 1P8M2T - 1.2V/3.3V [3]	5,020 [1]	4,460 [1]
UMC L65N Logic/Mixed-Mode LL [4]	9,720 [2]	9,140 [2]

Important notes: [1] Price = per block of 1525µm x 1525µm needed to fit the design in. Adding two blocks together to one block is possible.
[2] Price = per block of 1875µm x 1875µm needed to fit the design in. Adding two blocks together to one block is possible.

[3] UMC 0.18 and 0.13µ mini@sic rules

When the standard block of 5mm x 5mm is divided into 9 regular square sub-blocks, customers participating in the mini@sic program can submit one sub-block or multiple sub-blocks, depending on the size of their design:

- single sub-block: design may not be larger than 1525µm x 1525µm
- 2 sub-blocks: design may not be larger than 3240µm x 1525µm
- 3 sub-blocks: design may not be larger than 4960µm x 1525µm
- 4 sub-blocks: design may not be larger than 3240µm x 3240µm
- 6 sub-blocks: design may not be larger than 4960µm x 3240µm

Final price = number of sub-blocks needed to fit in the design * sub-block price.

[4] UMC 65nm mini@sic rules

For the mini@sic program, customers can submit one sub-block or multiple sub-blocks, depending on the size of their design:

- single sub-block: design may not be larger than 1875µm x 1875µm
- 2 sub-blocks: design may not be larger than 3950µm x 1875µm

X-FAB

Technology	Standard EUR / block	Discounted EUR / block
X-FAB XH018 0.18µ HV NVM CMOS E-FLASH (MET3, MET4, METMID, MET-THK)	4065	3750
X-FAB XT018 0.18µ HV SOI CMOS (MET3, MET4, METMID, METTHK)	4145	3825

Important notes: Price = per block of 1520µm x 1520µm needed to fit the design in. Adding two blocks together to one block is possible.