

ADC10b40MS180nm

10 Bit 40 MS/s Pipeline ADC

Key Parameters

- Resolution: 10 bit
- Conversion rate: up to 40 MS/s
- Power consumption: 30 mW @ 1.8 V
- Integral non-linearity: +/- 2.5 LSB
- Diff. non-linearity: +/- 1.0 LSB
- Supply voltage: 1.72 V – 1.88 V
- Operation clock: 1.0 – 40 MHz
- Input range: 0.53 V – 1.05 V
- Temperature range: -40 °C – 125 °C

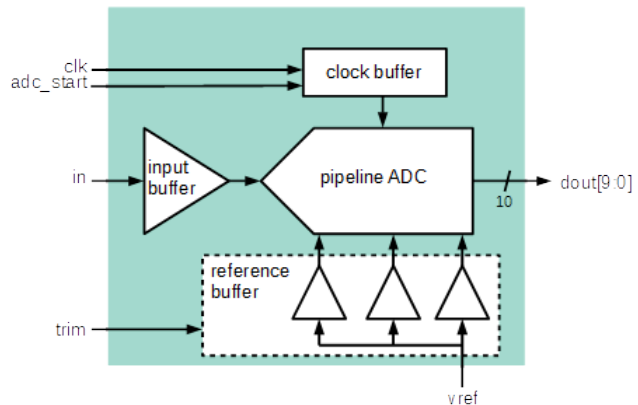


Fig. 1: IP-Level Block Diagram

General Description

The IP consists of a 10 bit 40 MS/s pipeline ADC. A time-interleaved architecture with 1.5 bit per stage is used. The operational amplifiers are shared between the interleaved stages for **reduced power consumption**. The interleaving is transparent for the application.

The latency of the ADC is 10 clock cycles. On the one hand, the ADC operation can be **triggered** using the `adc_start` input signal. On the other hand, **continuous conversion** of the input signal can be selected.

The integrated buffer provides a **high impedance input** in order to simplify the interface to the driving circuit. For low-power consumption a sample-and-hold-less architecture is used.

The reference drivers are included, which enables the operation using a **single reference voltage** e.g. a band-gap reference. 7 bit trimming of the reference is also included.

The ADC is **silicon proven** using the **AMS C18** process. Measurement results are available from evaluation and volume production. One application of the IP is an industrial sensor ASIC for safety critical applications.

Fraunhofer IIS provides a **detailed documentation** and **support** for the IP integration. **Modifications, extensions and technology ports** of the IP are available on request.

Benefits

- Low design risk due to silicon proven design
- Easy to use input due to integrated input buffer
- Robust operation across full temperature range from -40 °C up to 125 °C
- Simple integration due to integrated reference drivers and reference trimming DAC

Deliverables

- GDSII data
- Simulation model
- Documentation
- Silicon validation report
- Integration support

CONTACT

Fraunhofer IIS
 mixed-signal-ic-design@iis.fraunhofer.de