Fraunhofer
IIS

ADC12b020MS350nm

12 Bit 20 MS/s Pipeline ADC

Key Parameters

- Resolution: 12 bit
- Conversion rate: up to 20 MS/s
- Power consumption: 125 mW @ 3.3 V
- Integral non-linearity: +/- 2.0 LSB
- Diff. non-linearity: +/- 0.7 LSB
- Supply voltage: 3.0 V – 5.0 V
- Input voltage range: 0.5 - 2.3 V
- Operating temperature: 0 – 85 °C

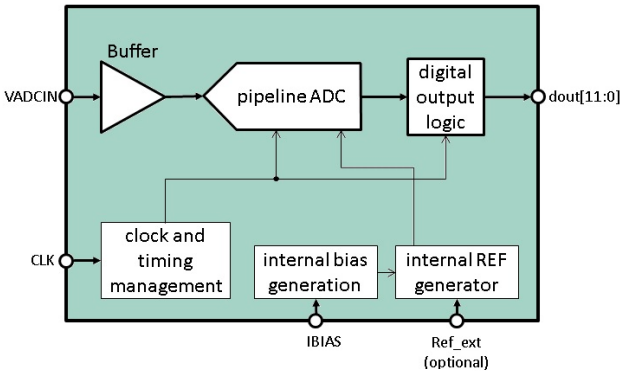

Fig. 1: IP-Level Block Diagram

General Description

This pipelined ADC can be applied for up to 20MSps sampling frequencies. By using interleaved switched-capacitor circuitries a CLK signal with half the sampling rate needs to be applied.

This ADC is built as a single-ended architecture and is designed to convert input signals from 0.5 – 2.3V at 3.3V supply voltage with up to 10 MHz input bandwidth with 12 bits resolution.

The ADC IP includes reference voltage generation with buffers and optional high-precision bandgap reference. The accuracy of the ADC is ensured by one-time-trimming of the reference voltages. Power-down mode is available.

The ADC is **silicon proven** using the **XFAB XH035** process. Measurement results and samples are available.

Fraunhofer IIS provides a **detailed documentation** and **support** for the IP integration. **Modifications, extensions and technology ports** of the IP are available on request.

Benefits

- Accelerated design service
- Design safety (first-time-right)
- Customer-specific flexible IPs
- Automated DfR and verification

Deliverables

- GDSII data
- Simulation model
- Documentation
- Integration and customizing support

FACT SHEET

CONTACT

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