ADC12b040MS180nm
12 Bit 40 MS/s Pipeline ADC

Key Parameters
- Resolution: 12 bit
- Conversion rate: 4 - 40 MS/s
- Power consumption: 95 mW @ 1.8 V
- Integral non-linearity: +/- 1.0 LSB
- Diff. non-linearity: +/- 0.8 LSB
- Supply voltage: 1.8 V
- Temperature range: -40 – 125°C
- Differential input: +/- 1.0 V

General Description
This pipelined ADC can be applied for up to 40MSps sampling rates with on-chip track&hold block or continuous signal sampling.

This fully differential ADC is designed to convert full swing (-1V to +1 V) input signals as well as unipolar input signals with 12 bits resolution. Furthermore the input voltage signals can exceed the 1.8V voltage range by using optional 3.3V input stage.

The ADC IP includes reference voltage generation and buffers and optional high-precision trimmed bandgap reference.

The ADC is silicon proven using the XFAB XH018 process. Measurement results and samples are available.

Fraunhofer IIS provides a detailed documentation and support for the IP integration. Modifications, extensions and technology ports of the IP are available on request.

Benefits
- Accelerated design service
- Design safety (first-time-right)
- Customer-specific flexible IPs
- Automated DfR and verification
- Seamless technology migration

Deliverables
- GDSII data
- Simulation model
- Documentation
- Integration and customizing support

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