ADC12b054kS180nm
12 Bit 54 kS/s Cyclic ADC

Key Parameters
- Resolution: 12 bit
- Conversion rate: up to 54 kS/s
- Power consumption: 370 μW @ 2.4 V
- Integral non-linearity: +/- 1.6 LSB
- Supply voltage: 2.4 V – 3.6 V
- Operation clock: up to 650 kHz
- Input voltage range: 1.9 V
- Operating temperature -40 – 125°C

General Description
This cyclic ADC, based on redundant-signed-digit (RSD) conversion, is optimized for sampling frequency and high accuracy. It provides 12 bit resolution for sampling frequencies up to 54 kS/s for continuous input signals.

This single ended ADC is designed to convert input signals with input swing of 1.9 V. The resolution is configurable (12 bit, 16 bit). Reference voltages can be generated on-chip or applied from outside.

The ADC IP includes serial-to-parallel interface (optional), reference voltage generation and buffers and high-precision trimmed bandgap reference (optional).

Different on-chip sensors (ambient light, temperature) and sensor frontends (instrumentation amplifier) are available.

The ADC is silicon proven using the XFAB XH018 process. Measurement results and samples are available.

Fraunhofer IIS provides a detailed documentation and support for the IP integration. Modifications, extensions and technology ports of the IP are available on request.

Benefits
- Accelerated design service
- Design safety (first-time-right)
- Customer-specific flexible IPs
- Automated DfR and verification
- Seamless technology migration

Deliverables
- GDSII data
- Simulation model
- Documentation
- Integration and customizing support

CONTACT
Fraunhofer IIS
mixed-signal-ic-design@iis.fraunhofer.de