

ADC15b008kS180nm

15 Bit 8 kS/s Sigma-Delta ADC

Key Parameters

- Resolution: 15 bit
- Conversion rate: 8 kSps
- Power consumption: 1.3 mW @ 1.8V
- ENOB: 14 bit
- Operation clock: 2.0 MHz
- Input voltage range: $\pm 1.0V$
- Operating temperature $-40 - 175^{\circ}C$

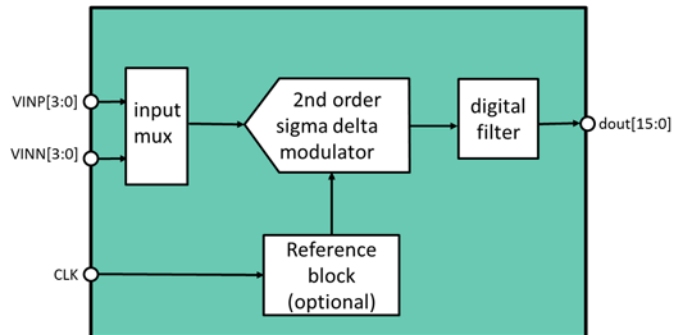


Fig. 1: IP-Level Block Diagram

General Description

The ADC IP is a general-purpose sigma-delta converter and it is configurable for conversion speed and power consumption with adaptable oversampling ratio.

It is built using typical second order architecture using correlated-double-sampling method. The target application is sampling of transient input voltages with 8kS/s with low-power and 192kS/s respectively.

The ADC IP includes reference voltage generation (optional) and 4-to-1 input multiplexer (optional) providing 4 differential input channels.

The ADC is **silicon proven and in mass production** using the **XFAB XH018** process. Measurement results and samples are available.

Fraunhofer IIS provides a **detailed documentation** and **support** for the IP integration.

Modifications, extensions and technology ports of the IP are available on request.

Benefits

- Accelerated design service
- Design safety (first-time-right)
- Customer-specific flexible IPs
- Automated DfR and verification
- Seamless technology migration

Deliverables

- GDSII data
- Simulation model
- Documentation
- Integration and customizing support

CONTACT

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