Fraunhofer
IIS

DAC12b001MS180nm

12 Bit 1 MS/s DAC with voltage output

Key Parameters

- Resolution: 12 bit
- Conversion rate: 1 MS/s
- Power consumption: 15 mW @ 3.3 V
- Integral non-linearity: +/- 1.5 LSB
- Diff. non-linearity: +/- 0.7 LSB
- Supply voltage: 3.0 V – 3.6 V
- Operation clock: 0 – 1 MHz
- Output voltage range: 1.8 V – 2.8 V
- Output load: >= 100 Ohm
- Temperature range: -40 °C – 125 °C

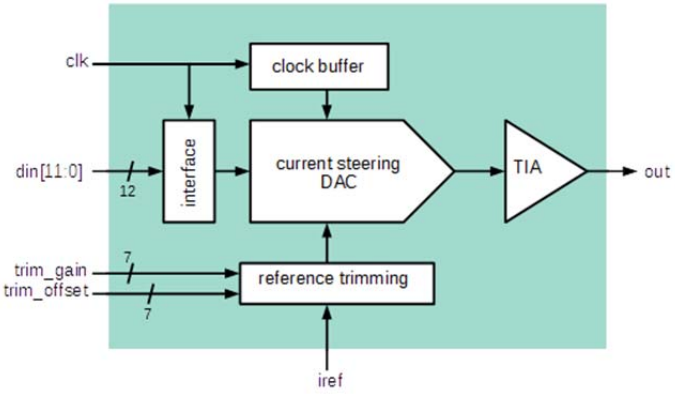

Fig. 1: IP-Level Block Diagram

General Description

The IP consists of a 12 bit **current steering DAC**. The DAC is connected to a **transimpedance amplifier** (TIA) in order to provide a voltage output signal. The amplifier can be adapted for different applications to optimize for performance, power consumption or output load of the IP.

The digital input data is saved to an **internal register** and provided immediately to the output.

The IP uses a **single current reference** input. A matching **current reference cell** can be provided. 7 bit gain and offset **trimming is included** to adapt for process variations.

The DAC is **silicon proven** using the **AMS C18** process. Measurement results are available from evaluation and volume production. One application of the IP is an industrial sensor ASIC for safety critical applications.

Fraunhofer IIS provides a **detailed documentation** and **support** for the IP integration. **Modifications, extensions and technology ports** of the IP are available on request.

Benefits

- Low design risk due to silicon proven design
- Easy to use input due to integrated output buffer
- Robust operation across full temperature range from -40 °C up to 125 °C
- Simple integration due to integrated reference drivers and reference trimming DAC

Deliverables

- GDSII data
- Simulation model
- Documentation
- Silicon validation report
- Integration support

FACT SHEET

CONTACT

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