General Description

The IP is a complete PLL including oscillator, loop filter, charge pump, phase detector and clock divider. The oscillator is realized as a differential ring oscillator, which enables a compact layout. The internal oscillator runs at 320 MHz.

The loop filter is completely integrated and, therefore, no external components are required. Decoupling capacitors are integrated for robust operation. The overall size of this IP block is 250 \( \mu \)m by 300 \( \mu \)m.

The PLL is designed for a temperature range from -40 \( ^\circ \)C up to 125 \( ^\circ \)C. A voltage regulator for the direct operation from 3.3 V or 5.0 V is available on request.

The PLL is silicon proven using the AMS C18 process. Measurement results are available from evaluation. One application of the IP is an industrial control ASIC.

Fraunhofer IIS provides a documentation and support for the IP integration. Modifications, extensions and technology ports of the IP are available on request.

Benefits

- Low design risk due to silicon proven design
- No external components due to integrated loop filter
- Improved testability of digital section due to bypass option
- Robust operation across full temperature range from -40 \( ^\circ \)C up to 125 \( ^\circ \)C

Deliverables

- GDSII data
- Simulation model
- Documentation
- Integration support