

# ADC12b002MS180nm

12 Bit 2 MS/s Sigma-Delta ADC

## Key Parameters

- Resolution: 12 - 14 bit
- Conversion rate: 20kS/s - 2 MSps
- Power consumption: 35 mW @ 1.8V
- Input voltage range: -2V ... 2V

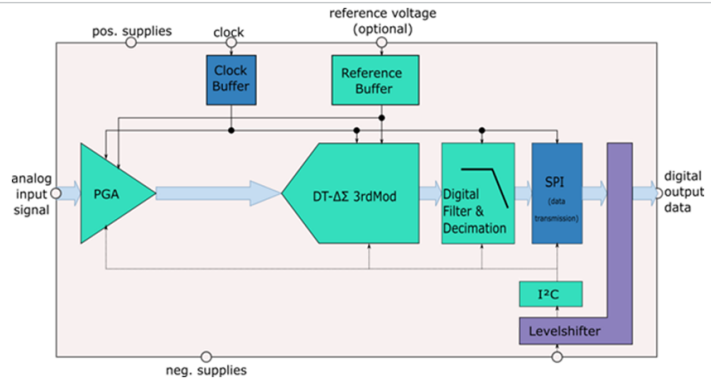


Fig. 1: IP-Level Block Diagram

## General Description

The ADC IP is a 3rd order sigma-delta converter including digital filter and decimation. It is configurable for conversion speed and power consumption.

The ADC IP includes reference voltage generation, CLK buffering and programmable gain amplification.

The ADC is **silicon evaluated** using the **XFAB XT018** process.

Fraunhofer IIS provides a **detailed documentation** and **support** for the IP integration.

**Modifications, extensions and technology ports** of the IP are available on request.

## Benefits

- Accelerated design service
- Design safety (first-time-right)
- Customer-specific flexible IPs
- Automated DfR and verification
- Seamless technology migration

## Deliverables

- GDSII data
- Simulation model
- Documentation
- Integration and customizing support

## CONTACT

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