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SDDAC16b008kS22nm

16-bit 8 kS/s Sigma-Delta DAC

Key Parameters

- Resolution: 16 bit
- Conversion rate: 8 kSps
- Power consumption: 0.3 mW @ 0.8 V
- SNR: 97.7 dB
- SFDR: 102.5 dB
- THD: -106.3 dB

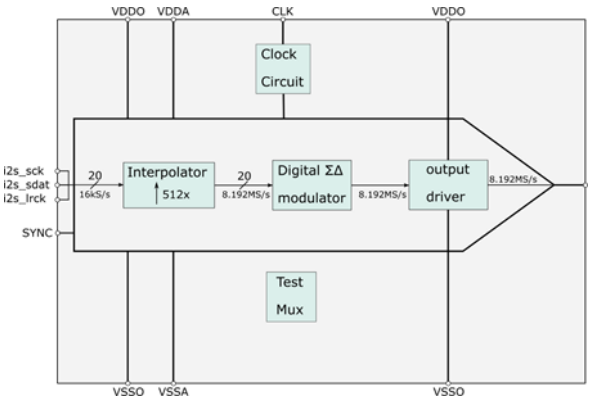


Fig. 1: IP-Level Block Diagram

General Description

The DAC IP is a Sigma-Delta Digital-to-Analog converter.

It consists of a second order digital delta sigma modulator, interpolation filter for overlampling as well as output driver, clock generation circuitry and test circuitry

The DAC is available as GDSII data for the **Globalfoundries 22nm FDX** process.
It is available for other process nodes (GF40nm, GF28SLP, XFAB180nm) on request.

Fraunhofer IIS provides a **detailed documentation** and **support** for the IP integration.
Modifications, extensions and technology ports of the IP are available on request.

Benefits

- Accelerated design service
- Design safety (first-time-right)
- Customer-specific flexible IPs
- Automated DfR and verification
- Seamless technology migration

Deliverables

- GDSII data
- Simulation model
- Documentation
- Integration and customizing support

FACT SHEET

CONTACT

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V1 (Q1/2026)